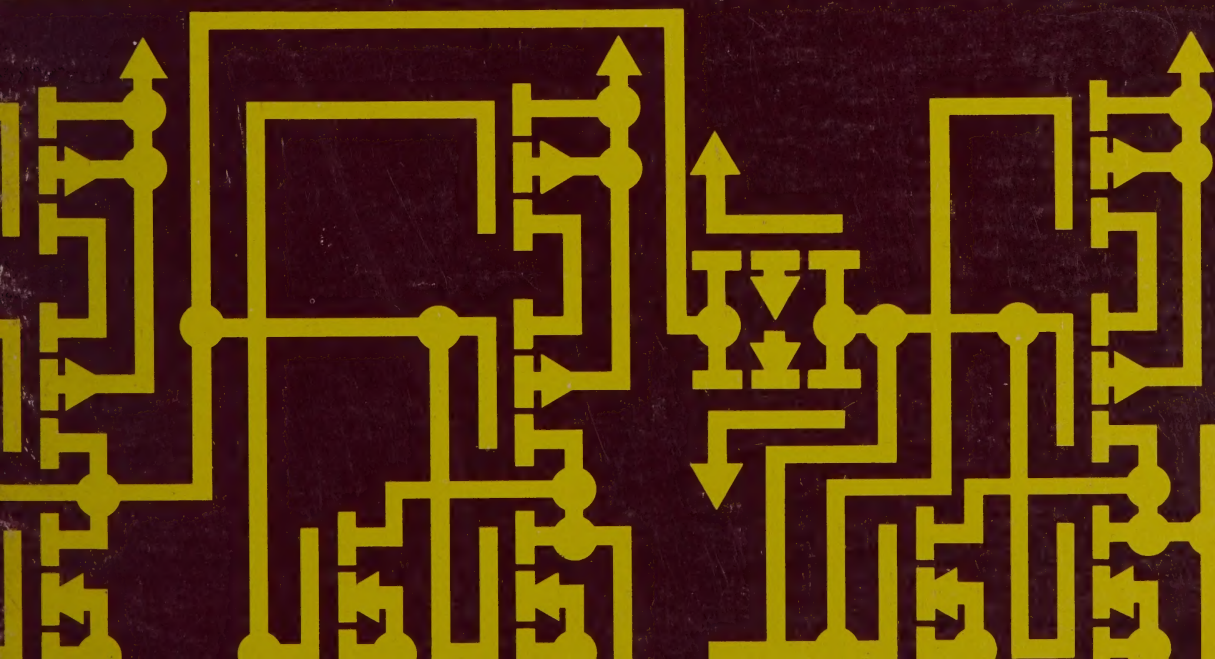
CMOS INTEGRATED CIRCUITS

DO NOT SELL

National



INTRODUCTION TO 74C

74C is a CMOS pin for pin, function for function, equivalent to the 7400 TTL family. This new concept in CMOS was designed with the engineer in mind. Strict design rules were adhered to in the input and output characteristics, such as making all outputs capable of sinking 360 μA (two LPT^{2}L loads) and specifying all AC parameters at 50 pF loads. These consistent design rules will simplify system design by giving the engineer realistic and workable parameters. The engineer can take full advantage of his knowledge of the 7400 line and utilize the design tricks he has learned.

For those designs that require 4000 Series, National manufactures these circuits as the 4600 Series.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

National does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied; and National reserves the right, at any time without notice, to change said circuitry.

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CMOS GUIDE

GATES

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MM74C02	Quad 2-Input NOR Gate
MM74C04	Hex Inverter
MM74C08	Quad 2-Input AND Gate
MM74C10	Triple 3-Input AND Gate
MM74C20	Dual 4-Input NAND Gate
MM74C30	8-Input NAND Gate
MM74C32	Quad 2-Input OR Gate
MM74C86	Quad 2-Input Exclusive OR Gate
MM4601A	Quad 2-Input NOR Gate
MM4602A	Dual 4-Input NOR Gate
MM4607A	Dual Complementary Pair Plus Inverter
MM4611A	Quad 2-Input NAND Gate
MM4612A	Dual 4-Input NAND Gate
MM4619A	Quad AND-OR Select Gate
MM4623A	Triple 3-Input NAND Gate
MM4625A	Triple 3-Input NOR Gate
MM4630A	Quad Exclusive OR Gate

BUFFERS

MM74C901	Hex Inverting TTL Buffer
MM74C902	Hex Non-Inverting TTL Buffer
MM74C903	Hex Inverting PMOS Buffer
MM74C904	Hex Non-Inverting PMOS Buffer
MM74C906	Open Drain Buffer (Active Pull Down)
MM74C907	Open Drain Buffer (Active Pull Up)
MM80C95	TRI-STATE® Hex Buffer
MM80C97	TRI-STATE® Hex Buffer
MM4609A	Hex Buffer (Inverting)
MM4610A	Hex Buffer
MM4649A	Hex Buffer (4609)
MM4650A	Hex Buffer (4610)

FLIP-FLOPS

MM74C73	Dual J-K Flip-Flop
MM74C74	Dual D Flip-Flop
MM74C76	Dual J-K Flip-Flop
MM74C107	Dual J-K Flip-Flop
MM74C173	TRI-STATE® Quad D Flip-Flop
MM74C174	Hex D Flip-Flop
MM74C175	Quad D Flip-Flop
MM4613A	Dual D Flip-Flop
MM4627A	Dual J-K Flip-Flop

COUNTERS

MM74C90	Decade Counter
MM74C93	Binary Counter
MM74C160	Sync Decade Counter
MM74C161	Sync Binary Counter

COUNTERS (CON'T)

MM74C162	Fully Sync Decade Counter
MM74C163	Fully Sync Binary Counter
MM74C192	Sync Up/Down Decade Counter
MM74C193	Sync Up/Down Binary Counter
MM4617A	Divide-by-10 Counter/Divider with 10 Decoded Outputs
MM4620A	14 Stage Ripple Carry Binary Counter/ Divider
MM4622A	Divide-by-8 Counter/Divider with 8 Decoded Outputs
MM4624A	Divide-by-8 Counter/Divider

SHIFT REGISTERS

MM74C95	4-Bit R-S L-S Register
MM74C164	8-Bit S-In P-Out Shift Register
MM74C165	8-Bit S-In P-Out Shift Register
MM74C195	4-Bit Parallel Shift Register
MM4606A	18-Bit Shift Register
MM4614A	8-Bit Static Shift Register
MM4621A	8-Bit Shift Register
MM4635A	4-Bit Parallel-In/Parallel-Out Shift Register

DECODERS/MULTIPLEXERS

MM74C42	BCD-to-Decimal Decoder
MM74C48	BCD-to-7 Segment Decoder
MM74C151	8 Channel Digital Multiplexer
MM74C154	4:16 Decoder/Demultiplexer
MM74C157	Quad 2-Input Multiplexer
MM4616A	Quad Bilateral Switch

MEMORIES

MM74C89	64-Bit TRI-STATE® Random Access Read/Write Memory
MM74C200	256-Bit TRI-STATE® Random Access Read/Write Memory

ARITHMETIC FUNCTIONS

MM74C83	4-Bit Binary Full Adder
MM74C85	4-Bit Magnitude Comparator

SPECIAL FUNCTIONS

MM74C14	Hex Schmitt Trigger
MM74C221	Dual Monostable Multivibrator
MM74C909	Linear Comparator
MM4616A	Quad Bilateral Switch

54C/74C POWER CONSUMPTION CHARACTERISTICS GUIDE

Typical characteristics $T_A = 25°C$.

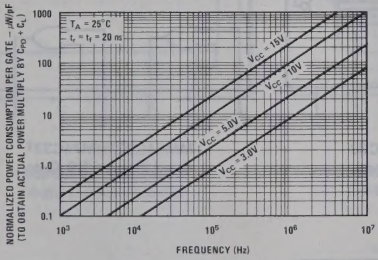
DEVICE TYPE/PRODUCT DESCRIPTION	C_{PD} (pF) (Note 3)	t_{pd} (ns) $C_L = 50$ pF $V_{CC} = 5.0V$	$\Delta t_{pd}/pF$ CURVE	LTTL (TTL)* FAN OUT
MM54C00/MM74C00 Quad 2-Input NAND Gate	12	50	A	2
MM54C02/MM74C02 Quad 2-Input NOR Gate	12	50	A	2
MM54C04/MM74C04 Hex Inverter	12	50	A	2
MM54C08/MM74C08 Quad 2-Input AND Gate	14	80	A	2
MM54C10/MM74C10 Triple 3-Input AND Gate	18	60	A	2
MM54C20/MM74C20 Dual 4-Input NAND Gate	30	70	A	2
MM54C30/MM74C30 8-Input NAND Gate	26	125	A	2
MM54C42/MM74C42 BCD-to-Decimal Decoder	50	200	A	2
MM54C73/MM74C73 Dual JK Flip-Flop	40	180	A	2
MM54C74/MM74C74 Dual D Flip-Flop	40	180	A	2
MM54C76/MM74C76 Dual JK Flip-Flop	40	180	A	2
MM54C83/MM74C83 4-Bit Binary Full Adder	120	300	A	2
MM54C85/MM74C85 4-Bit Magnitude Comparator	45	220 (1)	A	2
MM54C86/MM74C86 Quad 2-Input Exclusive OR Gate	20	110	A	2
MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Memory	230	270	A	2
MM54C95/MM74C95 4-Bit R-S/L-S Register	100	200	A	2
MM54C107/MM74C107 Dual JK Flip-Flop	40	180	A	2
MM54C151/MM74C151 8-Channel Digital Multiplexer	50	200 (1)	A	2
MM54C154/MM74C154 4:16 Decoder/Demultiplexer	60	275 (1)	A	2
MM54C157/MM74C157 Quad 2-Input Multiplexer	20	150 (1)	A	2
MM54C160/MM74C160 Sync Decade Counter	95	250 (2)	A	2
MM54C161/MM74C161 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C162/MM74C162 Sync Decade Counter	95	250 (2)	A	2
MM54C163/MM74C163 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C164/MM74C164 8-Bit SI/PO S/R	140	230 (2)	A	2
MM54C165/MM74C165 8-Bit PI/SO S/R	55	210 (2)	A	2
MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop	180	220 (2)	A	2
MM54C192/MM74C192 Sync Up/Down Decade Counter	70	250 (2)	A	2
MM54C193/MM74C193 Sync Up/Down Binary Counter	70	250 (2)	A	2
MM54C195/MM74C195 4-Bit Parallel S/R	130	200 (2)	A	2
MM54C901/MM74C901 Hex Inverting TTL Buffer	30	38	B	2*
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM54C903/MM74C903 Hex Inverting TTL Buffer	30	38	B	2*
MM54C904/MM74C904 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM70C95/MM80C95 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*
MM70C97/MM80C97 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*

Note 1: t_{pd} shown is from data input to output. For more detailed specifications see individual data sheet.

Note 2: t_{pd} shown is from clock to output. For more detailed specifications see individual data sheet.

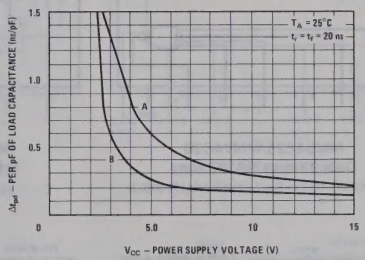
Note 3: C_{PD} numbers shown are for independent identical functions within a package. For instance the total C_{PD} for a MM75C157 is 4 x 20 pF = 80 pF while the total C_{PD} for the MM74C173 is 180 pF because all flip-flops have a common clock.

Normalized Typical Power Consumption vs Frequency



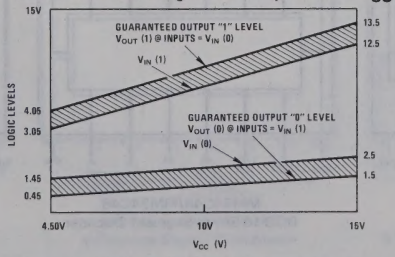
TOTAL POWER = $V_{CC}^2 \times f \times (C_{PD} + C_L) + V_{CC} I_{LEAKAGE}$

Typical Propagation Delay per pF of Load Capacitance vs Power Supply



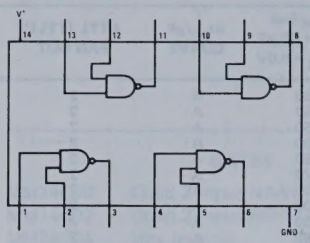
$$t_{pd}\Big|_{C_L = C} = (C - 50)\text{ pF} \times \frac{\Delta t_{pd}}{pF} + t_{pd}\Big|_{C_L = 50\text{ pF}}$$

Guaranteed Noise Margin Over Temperature vs V_{CC}

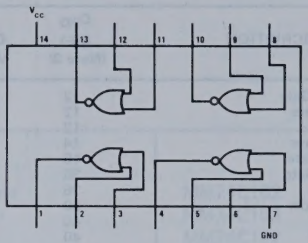


For complete explanation on use of curves see application note AN-90, 54C/74C Family Characteristics.

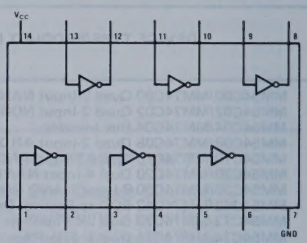
74C SERIES CMOS CONNECTION DIAGRAMS



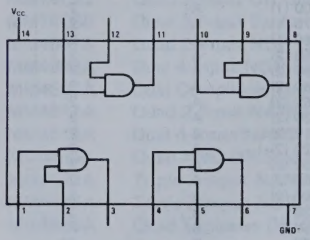
MM54C00/MM74C00
Quad 2-Input NAND Gate



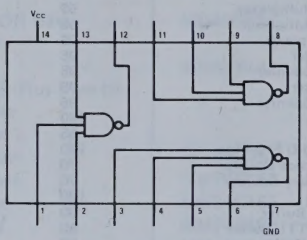
MM54C02/MM74C02
Quad 2-Input NOR Gate



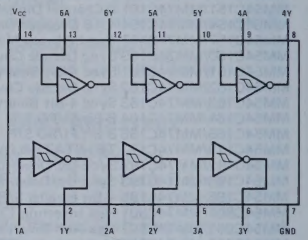
MM54C04/MM74C04
Hex Inverter



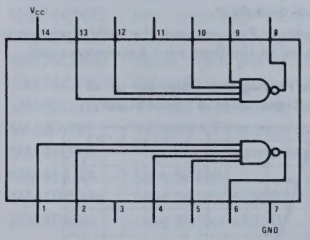
MM54C08/MM74C08
Quad 2-Input AND Gate



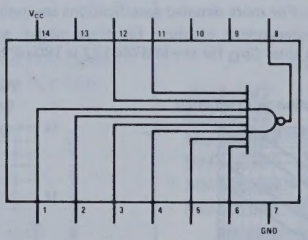
MM54C10/MM74C10
Triple 3-Input NAND Gate



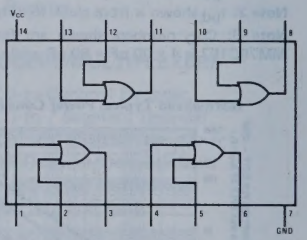
MM54C14/MM74C14†
Hex Schmitt Trigger



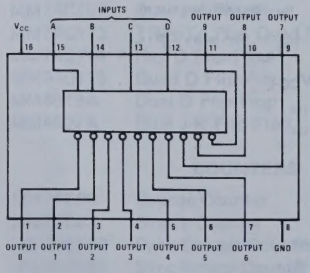
MM54C20/MM74C20
Dual 4-Input NAND Gate



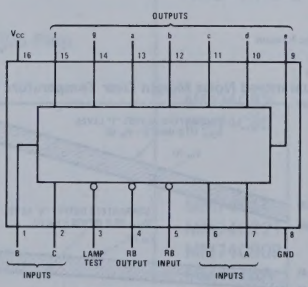
MM54C30/MM74C30
8-Input NAND Gate



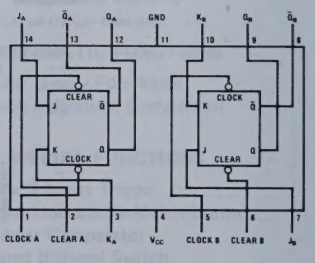
MM54C32/MM74C32†
Quad 2-Input OR Gate



MM54C42/MM74C42
BCD to Decimal Decoder



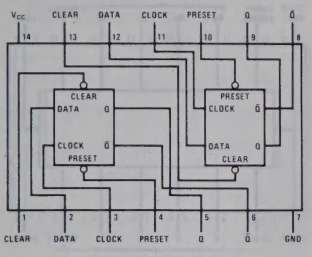
MM54C48/MM74C48
BCD to Seven Segment Decoder



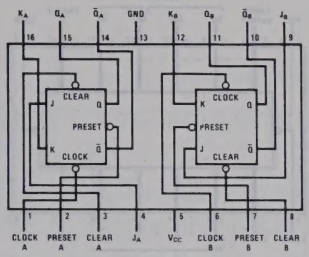
MM54C73/MM74C73
Dual J-K M/S Flip Flop

Note: All views are top views. †Devices under development.

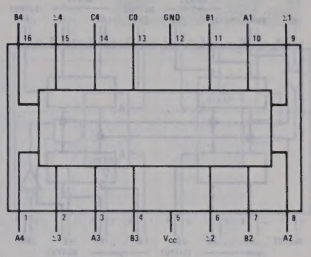
74C SERIES CMOS CONNECTION DIAGRAMS



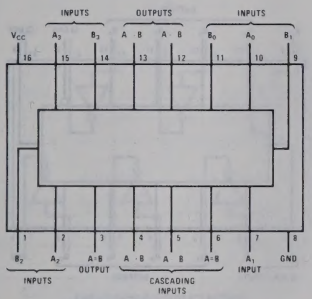
MM54C74/MM74C74
Dual D Flip-Flop



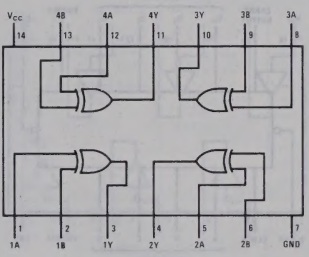
MM54C76/MM74C76
Dual J-K M/S Flip-Flop



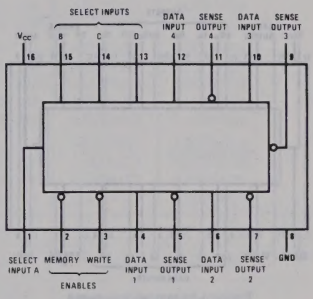
MM54C83/MM74C83
4-Bit Binary Full Adder


INPUTS OUTPUTS INPUTS
V_{CC} A_3 B_3 A=B A<B A>B B_0 A_0 B_1
16 15 14 13 12 11 10 9
B_2 A_2 A=B A<B A>B A=B A_1 GND
1 2 3 4 5 6 7 8
INPUTS OUTPUT CASCADING INPUTS INPUT

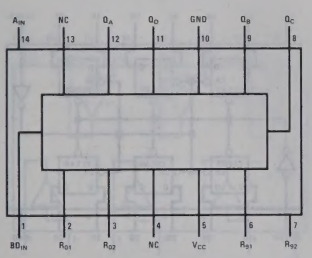
MM54C85/MM74C85
4-Bit Magnitude Comparator



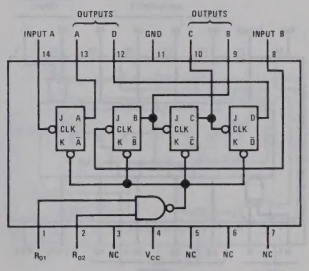
MM54C86/MM74C86
Quad 2-Input Exclusive OR Gate


SELECT INPUTS
V_{CC} B C D DATA INPUT 4 SENSE OUTPUT 4 DATA INPUT 3 SENSE OUTPUT 3
16 15 14 13 12 11 10 9
SELECT INPUT A MEMORY WRITE DATA INPUT 1 SENSE OUTPUT 1 DATA INPUT 2 SENSE OUTPUT 2 GND
1 2 3 4 5 6 7 8
ENABLES

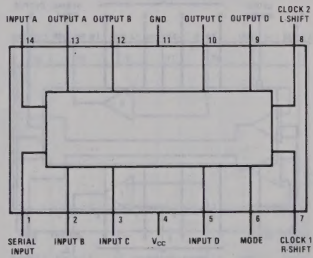
MM54C89/MM74C89
64-Bit RAM



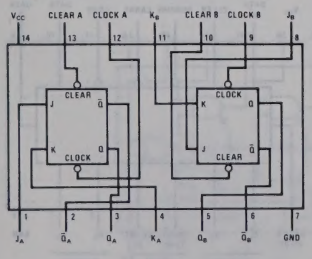
MM54C90/MM74C90†
4-Bit Decode Counter


OUTPUTS OUTPUTS
INPUT A A D GND C B INPUT B
14 13 12 11 10 9 8
J A CLK K $\bar{A}$ J B CLK K $\bar{B}$ J C CLK K $\bar{C}$ J D CLK K $\bar{D}$
R_{01} R_{02} NC V_{CC} NC NC NC
1 2 3 4 5 6 7

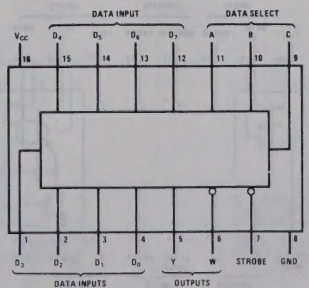
MM54C93/MM74C93†
4-Bit Binary Counter


INPUT A OUTPUT A OUTPUT B GND OUTPUT C OUTPUT D CLOCK 2 L-SHIFT
14 13 12 11 10 9 8
SERIAL INPUT INPUT B INPUT C V_{CC} INPUT D MODE CLOCK 1 R-SHIFT
1 2 3 4 5 6 7

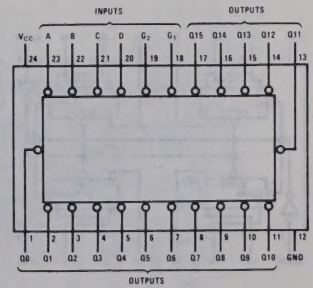
MM54C95/MM74C95
4-Bit Right-Shift Left-Shift Register



MM54C107/MM74C107
Dual J-K Flip-Flop

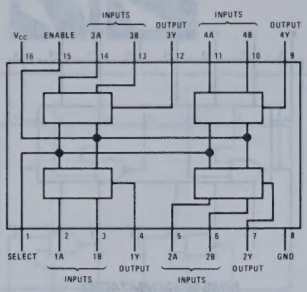


MM54C151/MM74C151
8-Channel Digital Multiplexer

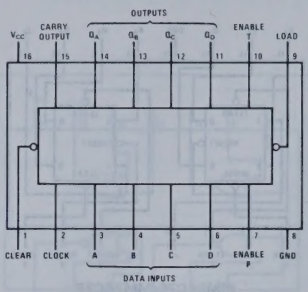


MM54C154/MM74C154
4 to 16 Line Decoder/Demultiplexer

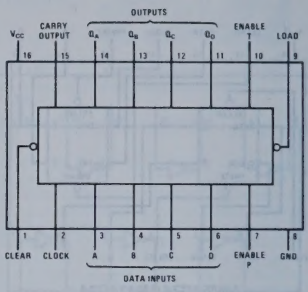
74C SERIES CMOS CONNECTION DIAGRAMS



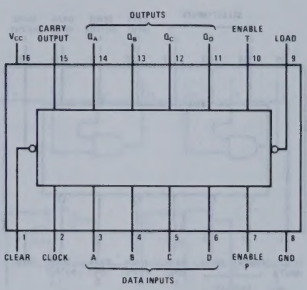
MM54C157/MM74C157
Quad 2-Input Multiplexer



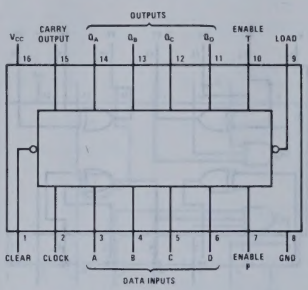
MM54C160/MM74C160
Asynchronous 4-Bit Decade Counter



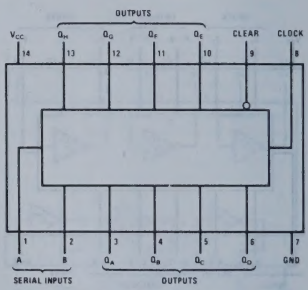
MM54C161/MM74C161
Asynchronous 4-Bit Binary Counter



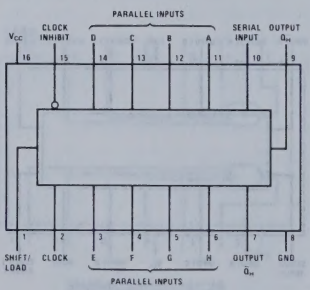
MM54C162/MM74C162
Synchronous 4-Bit Decade Counter



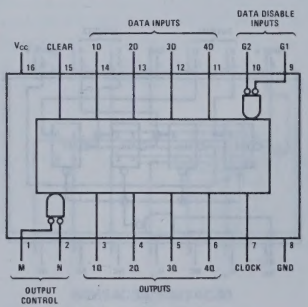
MM54C163/MM74C163
Synchronous 4-Bit Binary Counter



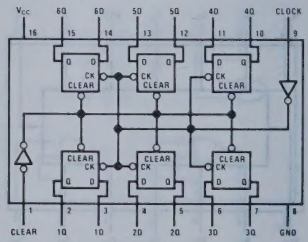
MM54C164/MM74C164
8-Bit Serial In/Parallel Out Shift Register



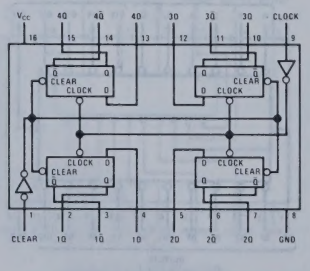
MM54C165/MM74C165
8-Bit Parallel In/Serial Out Shift Register



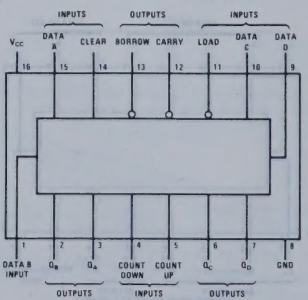
MM54C173/MM74C173
TRI-STATE® Quad D Flip-Flop
(Quad Latch)



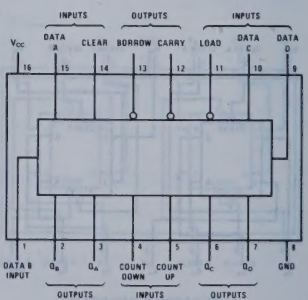
MM54C174/MM74C174
Hex D Flip-Flop



MM54C175/MM74C175†
Quad D Flip-Flop

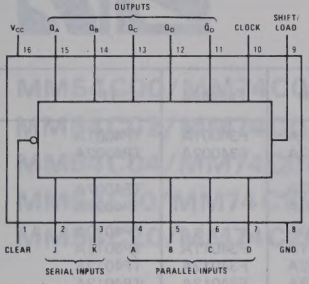


MM54C192/MM74C192
Synchronous Up/Down Decade Counter

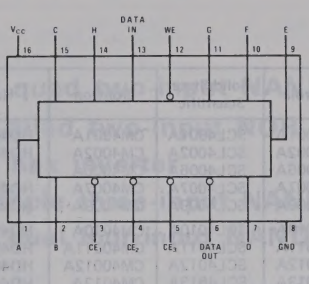


MM54C193/MM74C193
Synchronous Up/Down Binary Counter

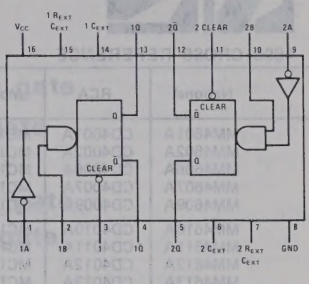
74C SERIES CMOS CONNECTION DIAGRAMS



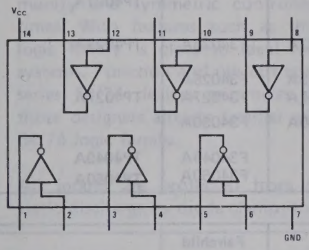
MM54C195/MM74C195
4-Bit Parallel Shift Register



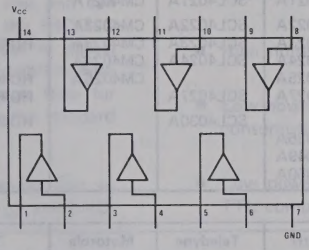
MM54C200/MM74C200†
256-Bit RAM



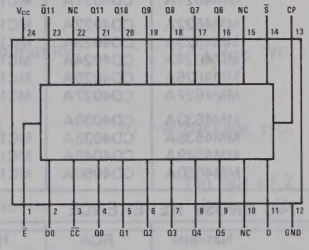
MM54C221/MM74C221†
Dual Monostable Multivibrator



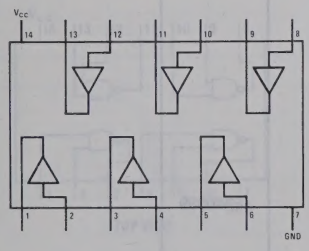
MM54C901/MM74C901
MM54C903/MM74C903
Hex Inverting Buffers



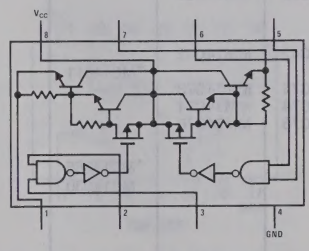
MM54C902/MM74C902
MM54C904/MM74C904
Hex Non-Inverting Buffers



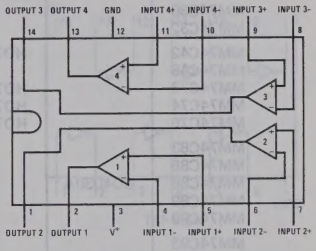
MM54C905/MM74C905†
12-Bit Successive Approximation Register



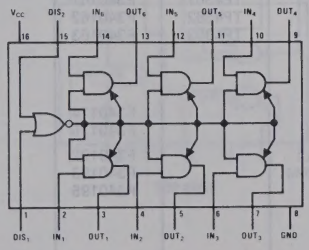
MM54C906/MM74C906
MM54C907/MM74C907
Hex Open Drain Buffers



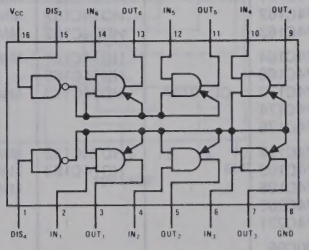
MM54C908/MM74C908†
Dual High Voltage CMOS Driver



MM54C909/MM74C909
Quad Comparator



MM70C95/MM80C95
TRI-STATE® Hex Non-Inverting Buffer



MM70C97/MM80C97
TRI-STATE® Hex Non-Inverting Buffer

CROSS REFERENCE GUIDE

4600 CROSS REFERENCE

National	RCA	Motorola	Solid State Scientific	Solitron	Harris	Fairchild	TI
MM4601A	CD4001A	MC14001A	SCL4001A	CM4001A	HD4001A	F34001A	TP4001A
MM4602A	CD4002A	MC14002A	SCL4002A	CM4002A	HD4002A	F34002A	TP4002A
MM4606A	CD4006A	MC14006A	SCL4006A	CM4006A			
MM4607A	CD4007A	MC14007A	SCL4007A	CM4007A	HD4007A		TP4007A
MM4609A	CD4009A	MC14009A	SCL4009A	CM4009A	HD4009A		TP4009A
MM4610A	CD4010A	MC14010A	SCL4010A	CM4010A	HD4010A		TP4010A
MM4611A	CD4011A	MC14011A	SCL4011A	CM40011A	HD4011A	F34011A	TP4011A
MM4612A	CD4012A	MC14012A	SCL4012A	CM40012A	HD4012A	F34012A	TP4012A
MM4613A	CD4013A	MC14013A	SCL4013A	CM4013A	HD4013A	F34013A	TP4013A
MM4614A	CD4014A		SCL4014A	CM4014A			TP4014A
MM4616A	CD4016A	MC14016A	SCL4016A	CM4016A			TP4016A
MM4617A	CD4017A	MC14017A		CM4017A			
MM4619A	CD4019A		SCL4019A	CM40019A	HD4019A	F34019A	TP4019A
MM4620A	CD4020A	MC14020A	SCL4020A	CM4020A			
MM4621A	CD4021A	MC14021A	SCL4021A	CM4021A			TP4021A
MM4622A	CD4022A	MC14022A	SCL4022A	CM4022A			
MM4623A	CD4023A	MC14023A	SCL4023A	CM4023A	HD4023A	F34023A	TP4023A
MM4624A	CD4024A	MC14024A	SCL4024A	CM4024A			
MM4625A	CD4025A	MC14025A		CM4025A	HD4025A	F34025A	
MM4627A	CD4027A	MC14027A	SCL4027A		HD4027A	F34027A	TP4027A
MM4630A	CD4030A		SCL4030A		HD4030A	F34030A	
MM4635A	CD4035A	MC14035A					
MM4649A	CD4049A	MC14049A				F34049A	TP4049A
MM4650A	CD4050A	MC14050A				F34050A	TP4050A

74C CROSS REFERENCE

National	RCA	Harris	Teledyne	Motorola	TI	Fairchild	
MM74C00		HD74C00	MM74C00				
MM74C02		HD74C02	MM74C02				
MM74C04	CD4069A	HD74C04	MM74C04				
MM74C08							
MM74C10		HD74C10	MM74C10				
MM74C14							
MM74C20		HD74C20	MM74C20				
MM74C30							
MM74C32							
MM74C42		HD74C42	MM74C42				
MM74C48				*MC14511			
MM74C73		HD74C73	MM74C73				
MM74C74		HD74C74	MM74C74				
MM74C76		HD74C76	MM74C76				
MM74C83							
MM74C85				*MC14585			
MM74C86	CD4030A			MC14030			
MM74C89						F340089	
MM74C90							
MM74C93							
MM74C95			MM74C95				
MM74C107		HD74C107					
MM74C151		HD74C151	MM74C151				
MM74C154		HD74C154	MM74C154				
MM74C157		HD74C157	MM74C157				
MM74C160		HD74C160	MM74C160		TP4360	F340160	
MM74C161		HD74C161	MM74C161		TP4361	F340161	
MM74C162		HD74C162	MM74C162		TP4362	F340162	
MM74C163		HD74C163	MM74C163		TP4363	F340163	
MM74C164		HD74C164	MM74C164				
MM74C165		HD74C165					
MM74C173	CD4076A	HD74C173	MM74C173				
MM74C174						F340174	
MM74C175						F340175	
MM74C192		HD74C192	MM74C192			F340192	
MM74C193		HD74C193	MM74C193			F340193	
MM74C195			MM74C195			F340195	
MM74C200							
MM74C221							
MM80C95							
MM80C97						F340097	
MM80C98						F340098	

*Functional equivalents.

MM54C00/MM74C00 quad two-input NAND gate
MM54C02/MM74C02 quad two-input NOR gate
MM54C04/MM74C04 hex inverter
MM54C10/MM74C10 triple three-input NAND gate
MM54C20/MM74C20 dual four-input NAND gate

general description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

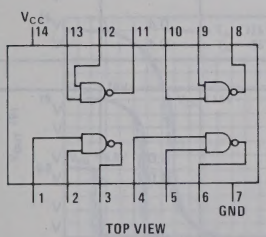
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power consumption	10 nW/package typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

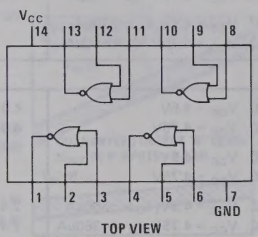
connection diagrams

MM54C00/MM74C00



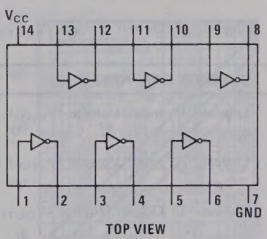
TOP VIEW

MM54C02/MM74C02



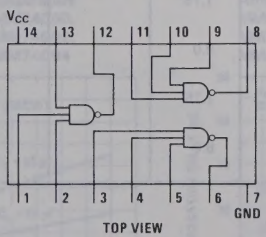
TOP VIEW

MM54C04/MM74C04



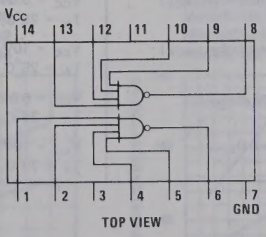
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
54C	$-55^{\circ}C$ to $+125^{\circ}C$
74C	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

dc electrical characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10V$, $I_O = -10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$ $V_{CC} = 10V$, $I_O = +10\mu A$			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.01	15	μA
LOW POWER TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -10\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -10\mu A$	4.4 4.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = +10\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = +10\mu A$			0.4 0.4	V V
CMOS TO LOW POWER					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	4.0 4.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			1.0 1.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$ 74C, $V_{CC} = 4.75$, $I_O = 360\mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	$V_{CC} = 5.0V$, $V_{IN(0)} = 0V$ $T_A = 25^{\circ}C$, $V_{OUT} = 0V$	1.75			mA
Output Source Current (I_{SOURCE})	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25^{\circ}C$, $V_{OUT} = 0V$	8.0			mA
Output Sink Current (I_{SINK})	$V_{CC} = 5.0V$, $V_{IN(1)} = 5.0V$ $T_A = 25^{\circ}C$, $V_{OUT} = V_{CC}$	1.75			mA
Output Sink Current (I_{SINK})	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25^{\circ}C$, $V_{OUT} = V_{CC}$	8.0			mA

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		50	90	ns
	V_{CC} = 10V		30	60	ns
Input Capacitance (C_{IN})	(Note 2)		6.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		60	100	ns
	V_{CC} = 10V		35	70	ns
Input Capacitance (C_{IN})	(Note 2)		7.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		18		pF
MM54C20/MM74C20					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		70	115	ns
	V_{CC} = 10V		40	80	ns
Input Capacitance (C_{IN})	(Note 2)		9		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		30		pF

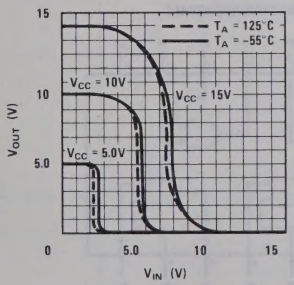
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

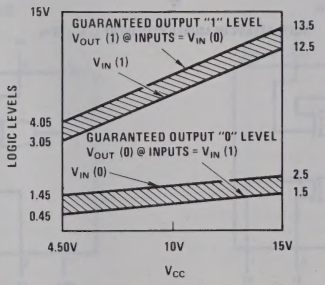
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90

typical performance characteristics

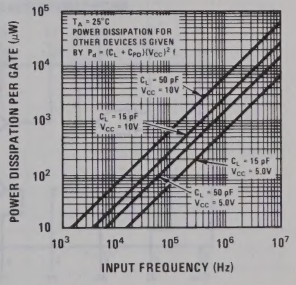
Gate Transfer Characteristics



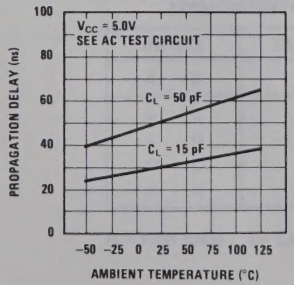
Guaranteed Noise Margin Over Temperature vs V_{CC}



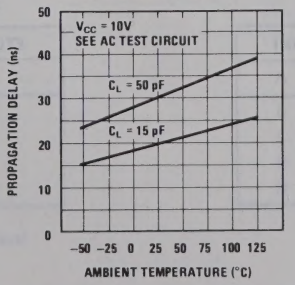
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



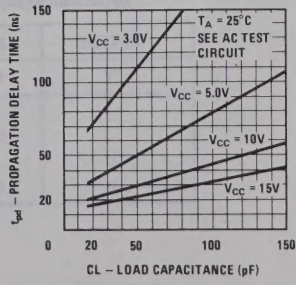
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

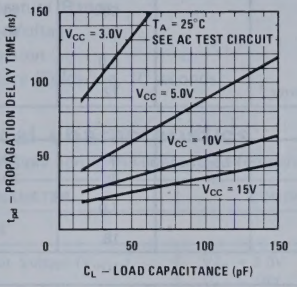


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

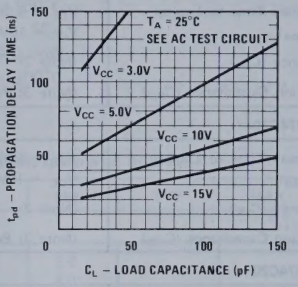


typical performance characteristics (con't)

Propagation Delay Time vs
Load Capacitance
MM54C10/MM74C10

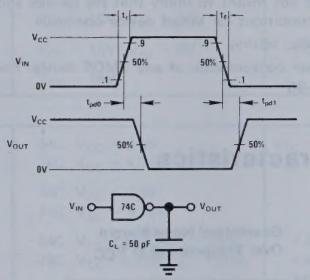


Propagation Delay Time vs
Load Capacitance
MM54C20/MM74C20



switching time waveforms and ac test circuits

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

MM54C08/MM74C08 quad 2-input AND gate
MM54C86/MM74C86 quad 2-input EXCLUSIVE-OR gate

general description

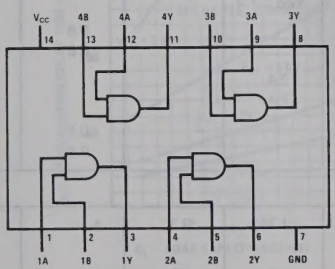
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enchancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Low power consumption — 10 nW/package typ

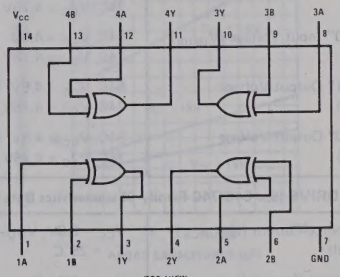
connection diagrams

Dual-In-Line Package
MM54C08/MM74C08



TOP VIEW

Dual-In-Line Package
MM54C86/MM74C86



TOP VIEW

truth tables

MM54C86/MM74C86

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L= Low Level

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C08, MM54C86	−55°C to +125°C
MM74C08, MM74C86	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics

(MM54C08/MM74C08) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		80 40	140 70	ns ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3		14		pF

ac electrical characteristics

(MM54C86/MM74C86) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 50	185 90	ns ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3		20		pF

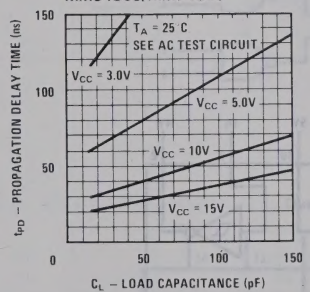
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

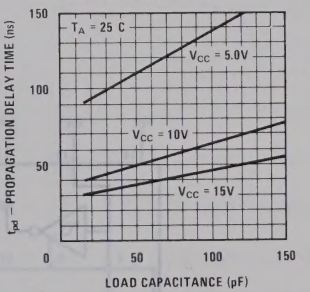
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

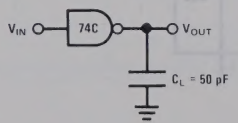
Propagation Delay Time vs Load Capacitance MM54C08/MM74C08



Propagation Delay Time vs Load Capacitance MM54C86/MM74C86

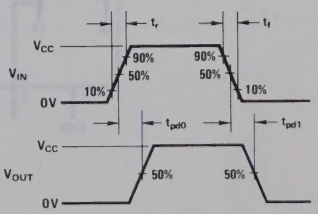


ac test circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

switching time waveforms



Advance Information

MM54C14/MM74C14 hex schmitt trigger

general description

The MM54C14/MM74C14 Hex Schmitt trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors.

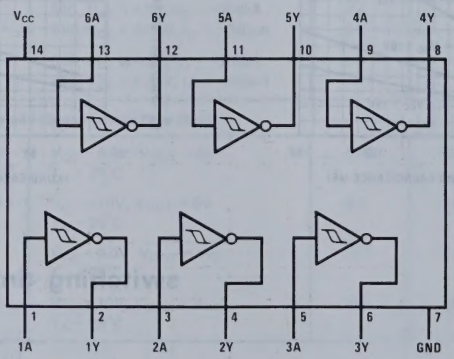
features

- Wide supply voltage range — 3.0 V to 15 V
- Low power T^2L compatible — drive 2 LT^2L loads

application

- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

connection diagram



TOP VIEW

MM54C14/MM74C14
Hex Schmitt Trigger

MM54C30/MM74C30 8-input NAND gate

general description

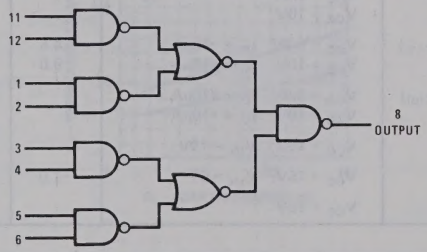
The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

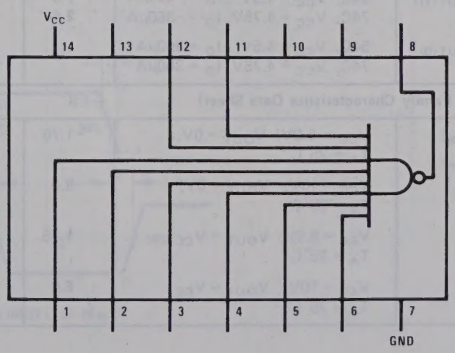
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C30	$-55°C$ to $+125°C$
MM74C30	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	$300°C$

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10V$, $I_O = -10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$ $V_{CC} = 10V$, $I_O = +10\mu A$			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$, $T_A = 25°C$	-1.75	-3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	-8.0	-15		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8.0	16		mA

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		125 55	180 90	ns ns
Input Capacitance (C_{IN})	(Note 2)		4.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Gate		26		pF

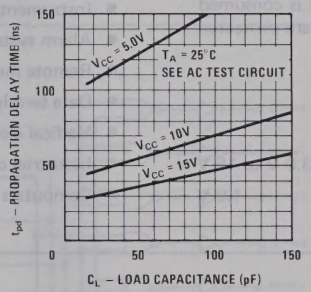
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

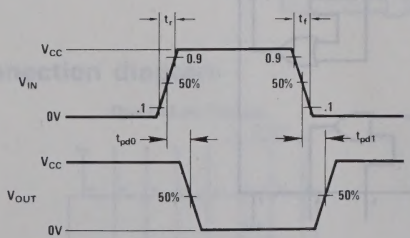
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

Propagation Delay Time vs Load Capacitance

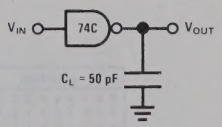


switching time waveforms



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns.

ac test circuit



Advance Information

MM54C32/MM74C32 quad 2-input OR gate

general description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

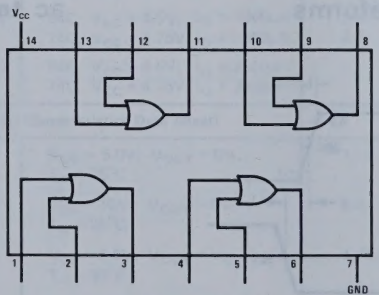
features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} typ
■ Low power	10 nW typ
■ Low power T^2L compatible	drive 2 LT^2L loads

application

- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

connection diagram



MM54C32/MM74C32
Quad 2-Input OR Gate

MM54C42/MM74C42 BCD to decimal decoder

general description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

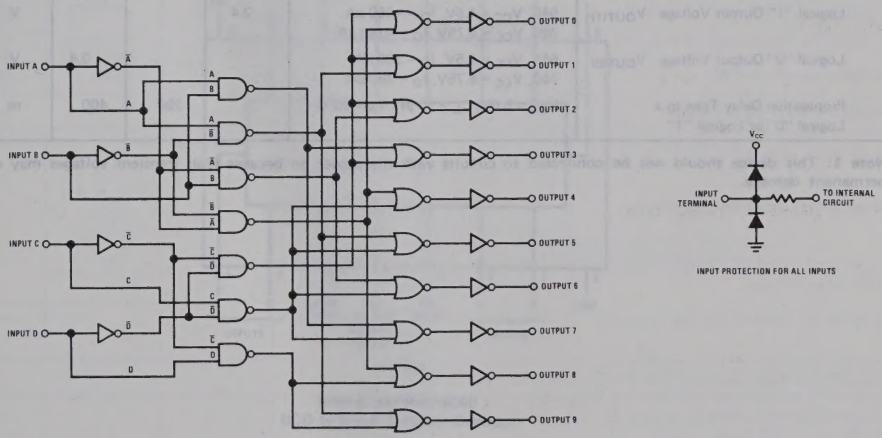
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V V_{CC}

applications

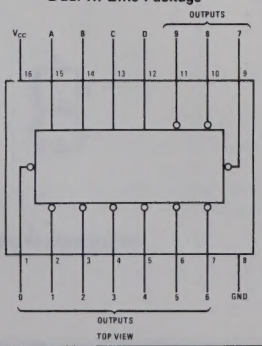
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

schematic diagram



connection diagram

Dual-In-Line Package



truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$	Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM54C42	$-55^{\circ}C$ to $+125^{\circ}C$	Package Dissipation	500 mW
MM74C42	$0^{\circ}C$ to $+70^{\circ}C$	Operating V_{CC} Range	3V to 15V
Maximum V_{CC} Voltage	16V	Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10.0V$	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10.0V$			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC}=5.0V$, $I_O=-10\,\mu A$	4.5			V
		$V_{CC}=10.0V$, $I_O=-10\,\mu A$	9.0			V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC}=5.0V$, $I_O=+10\,\mu A$			0.5	V
		$V_{CC}=10.0V$, $I_O=+10\,\mu A$			1	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{CC}=15.0V$, $V_{IN}=15V$			1	μA
Logical "0" Input Current	$I_{IN(0)}$	$V_{CC}=15.0V$, $V_{IN}=0V$	-1			μA
Supply Current	I_{CC}	$V_{CC}=15.0V$		0.05	300	μA
Input Capacitance		Any Input		5		pF
Propogation Delay Time to a Logical "0" or Logical "1"		$V_{CC}=5.0V$, $C_L=50$ pF, $T_A=25^{\circ}C$		200	300	ns
		$V_{CC}=10.0V$, $C_L=50$ pF, $T_A=25^{\circ}C$		90	140	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, $V_{CC}=4.5V$, $I_O=-360\,\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\,\mu A$				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, $V_{CC}=4.5V$, $I_O=360\,\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\,\mu A$				
Propagation Delay Time to a Logical "0" or Logical "1"		$V_{CC}=5.0V$, $C_L=50$ pF, $T_A=25^{\circ}C$		250	400	ns

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

Advance Information

MM54C48/MM74C48 BCD-to-7 segment decoder

general description

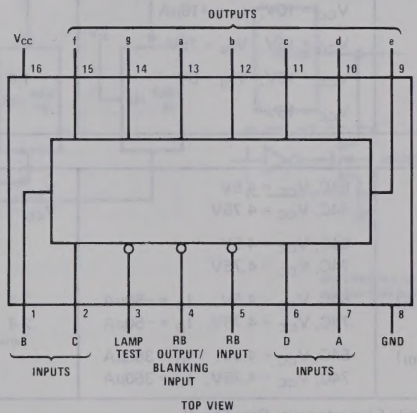
The MM54C48/MM74C48 BCD to 7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power — fan out of 2
  TTL compatibility — driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

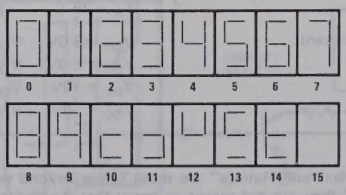
connection diagram

Dual-In-Line Package



MM54C48/MM74C48
BCD to Seven Segment Decoder

Segment Identification



Numerical Designations and Resultant Displays

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C48	−55°C to +125°C
MM74C48	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
(RB Output Only)	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −50μA	2.4			V
(RB Output Only)	74C, V_{CC} = 4.75V, I_O = −50μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel) (RB Output Only)	V_{CC} = 4.75V, V_{OUT} = 0.4V			−0.80	mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Output Source Current (NPN Bipolar)	V_{CC} = 5.0V, V_{OUT} = 3.4	20	50		mA
	V_{CC} = 5.0V, V_{OUT} = 3.0		65		mA
	V_{CC} = 10V, V_{OUT} = 8.4	20	50		mA
	V_{CC} = 10V, V_{OUT} = 8.0		65		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

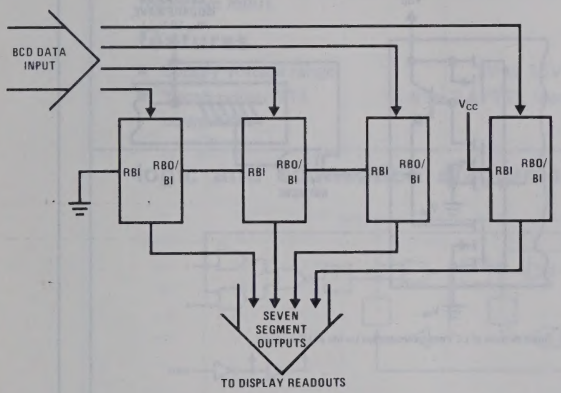
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics $T_A = 25^\circ C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$	450	1500		ns
	$V_{CC} = 10V$	160	500		ns
Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$	500	1600		ns
	$V_{CC} = 10V$	180	550		ns
Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$	350	1200		ns
	$V_{CC} = 10V$	140	450		ns
Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$	450	1500		ns
	$V_{CC} = 10V$	160	500		ns
Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$	600	2000		ns
	$V_{CC} = 10V$	250	800		ns
Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$	140	450		ns
	$V_{CC} = 10V$	50	150		ns

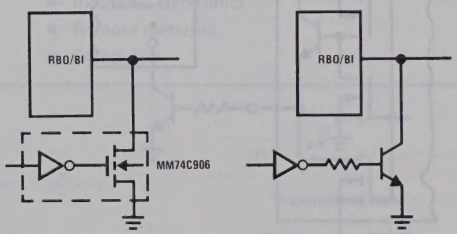
typical applications

Typical Connection Utilizing the Ripple-Blanking Feature



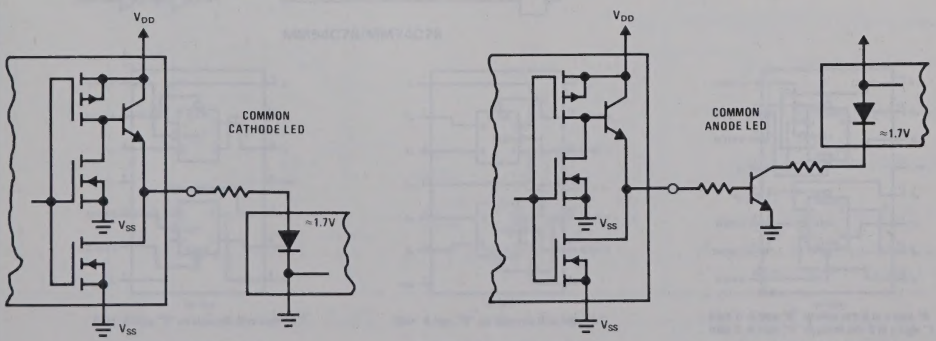
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

Blanking Input Connection Diagram



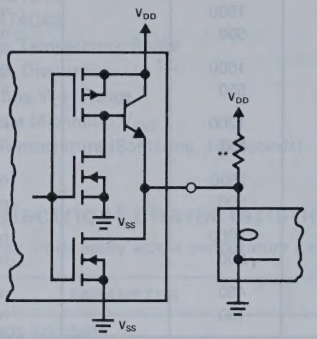
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout



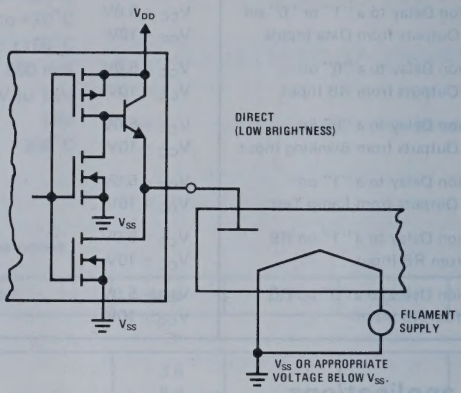
typical applications (con't)

Incandescent Readout

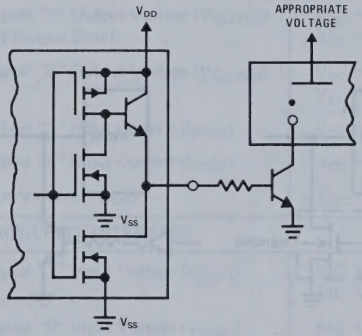


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

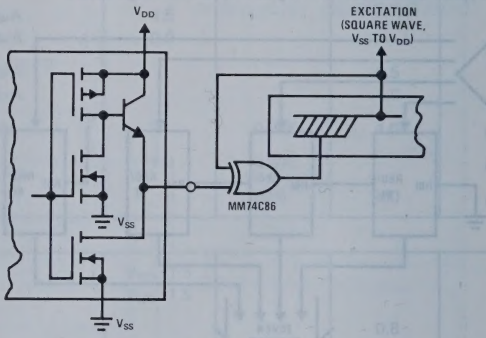
Fluorescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

MM54C73/MM74C73 dual J-K flip-flops with clear
MM54C76/MM74C76 dual J-K flip-flops with clear and preset
MM54C107/MM74C107 dual J-K flip-flops with clear

general description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

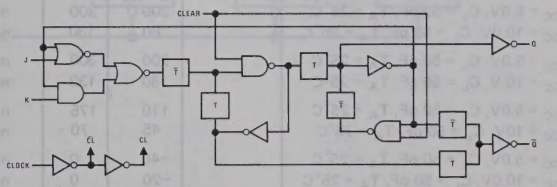
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — 50 nW (typ)
- Medium speed operation — 10 MHz (typ) with 10V supply

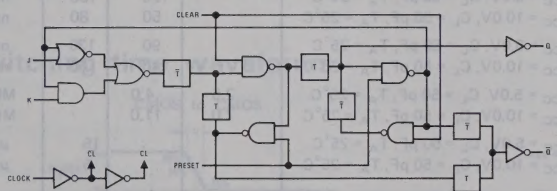
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams

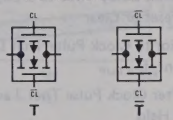


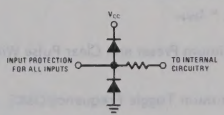
MM54C73/MM74C73 and MM54C107/MM74C107

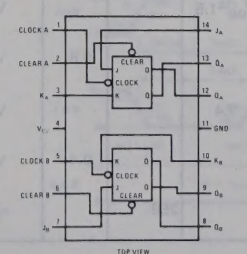


MM54C76/MM74C76

Transmission Gate

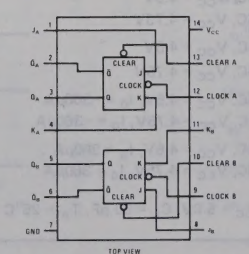






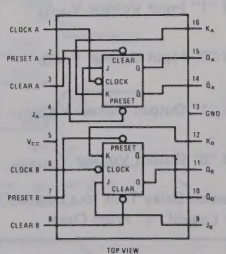
Note: A logic "0" on clear sets Q to logic "0."

MM54C73/MM74C73



Note: A logic "0" on clear sets Q to logic "0."

MM54C107/MM74C107



Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

MM54C76/MM74C76

absolute maximum ratings

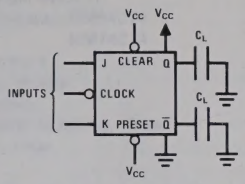
Voltage at any pin (Note 1)	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature MM54CXX	$-55^\circ C$ to $125^\circ C$
MM74CXX	$0^\circ C$ to $70^\circ C$
Storage Temperature	$-65^\circ C$ to $150^\circ C$
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	$300^\circ C$
Operating V_{CC} Range	+3V to 15V

electrical characteristics

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10.0V$	8			V
Logical "0" Input Voltage $V_{IN(0)}$	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10.0V$			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	$V_{CC} = 5.0V$	4.5			V
	$V_{CC} = 10.0V$	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	$V_{CC} = 5.0V$			0.5	V
	$V_{CC} = 10.0V$			1.0	V
Logical "1" Input Current $I_{IN(1)}$	$V_{CC} = 15.0V$			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	$V_{CC} = 15.0V$	-1.0			μA
Supply Current I_{CC}	$V_{CC} = 15.0V$		0.050	60	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		180	300	ns
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		70	110	ns
Propagation Delay Time to a Logical "0" From Preset or Clear	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		200	300	ns
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		80	130	ns
Propagation Delay Time to a Logical "1" From Preset or Clear	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		200	300	ns
	$V_{CC} = 10.V$, $C_L = 50$ pF, $T_A = 25^\circ C$		80	130	ns
Time Prior to Clock Pulse That Data Must be Present, t_{SETUP}	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		110	175	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25^\circ C$		45	70	ns
Time After Clock Pulse That J and K Must be Held	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		-40	0	ns
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		-20	0	ns
Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		120	190	ns
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		50	80	ns
Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		90	130	ns
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		40	60	ns
Maximum Toggle Frequency	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$	2.5	4.0		MHz
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$	7.0	11.0		MHz
Clock Pulse Rise and Fall Time	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$			15	μs
	$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$			5	μs
LOW POWER TTL TO CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, $V_{CC} = 4.5V$				
	74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Votlage $V_{IN(0)}$	54C, $V_{CC} = 4.5V$				
	74C, $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, $V_{CC} = 4.5V$, $I_0 = -360\mu A$				
	74C, $V_{CC} = 4.75V$, $I_0 = -360\mu A$	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, $V_{CC} = 4.5V$, $I_0 = 360\mu A$				
	74C, $V_{CC} = 4.75V$, $I_0 = 360\mu A$			0.4	V
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" From Clock	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^\circ C$		250		ns

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac test circuit



truth table

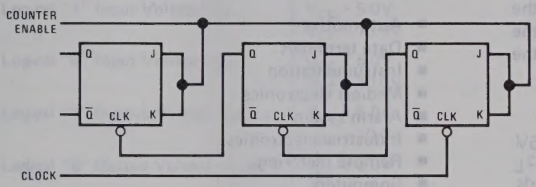
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse.

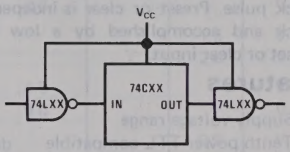
t_{n+1} = bit time after clock pulse.

typical applications

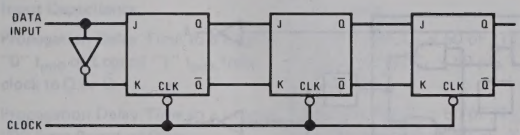
Ripple Binary Counters



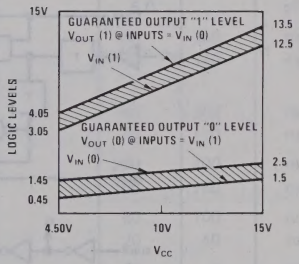
74C Compatibility



Shift Registers

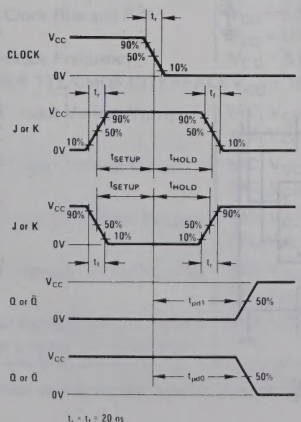


Guaranteed Noise Margin as a Function of V_{CC}



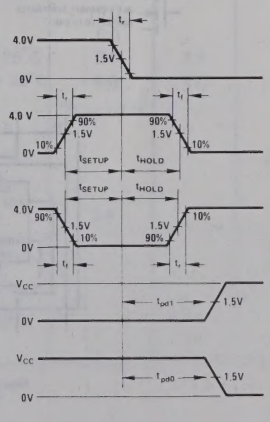
switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

TTL to CMOS



MM54C74/MM74C74 dual D flip-flop

general description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

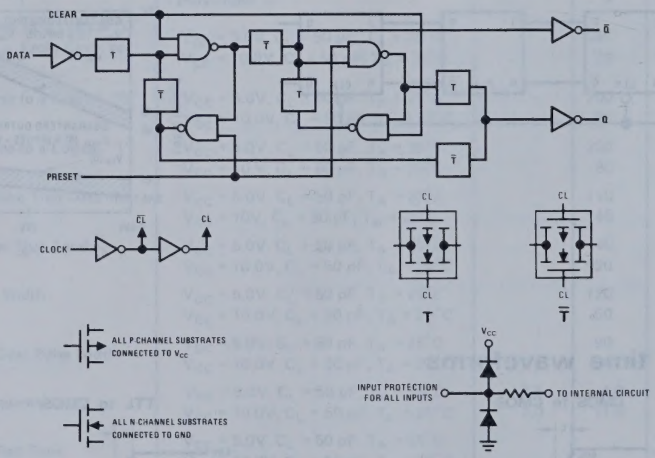
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

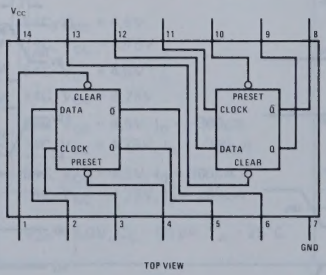
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Note: A logic "0" on clear sets Q to logic "0."
A logic "0" on preset sets Q to logic "1."

absolute maximum ratings

Voltage at any pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating temperature MM54C74	−55°C to 125°C
MM74C74	0°C to 70°C
Storage temperature	−65°C to 150°C
Maximum V_{CC} Voltage	16V
Package dissipation	500 mW
Lead temperature (Soldering, 10 sec)	300°C
Operating V_{CC} range	+3V to +15V

electrical characteristics

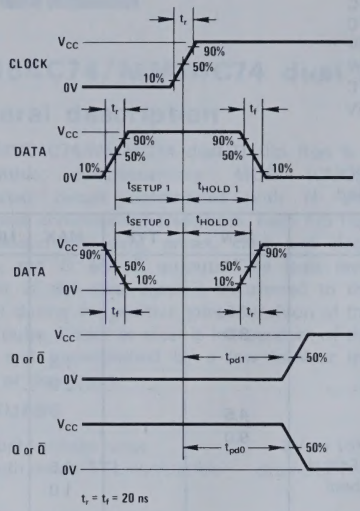
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	60	μA
Input Capacitance	Any Input		5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "0" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "1" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100	150	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		50	100	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		20	40	ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		−20	0	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−8.0	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40		ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	160	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40	70	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	15.0			μs
	V_{CC} = 10.0V, C_L = 50 pF	5.0			μs
Maximum Clock Frequency	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	2.0	3.5		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	5.0	8.0		MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.75V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = − 360 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = − 360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.50V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" from clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250		V

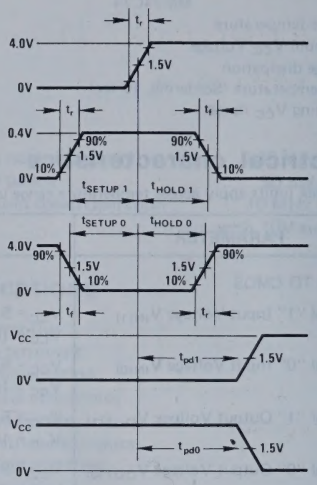
Note 1: These devices should not be connected under power on conditions.

switching time waveforms

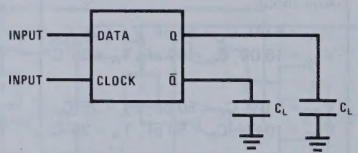
CMOS to CMOS



TTL to CMOS

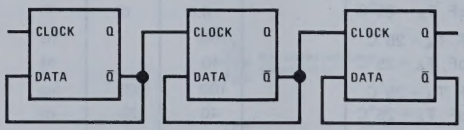


ac test circuit

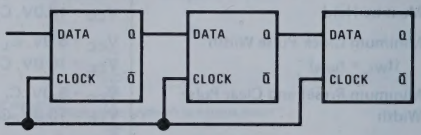


typical applications

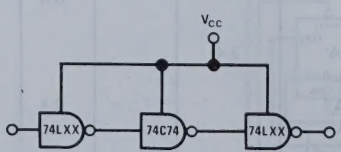
Ripple Counter (Divide by 2^n)



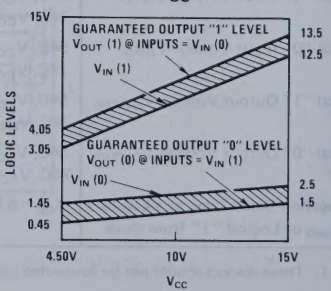
Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



MM54C83/MM74C83 4-bit binary full adder

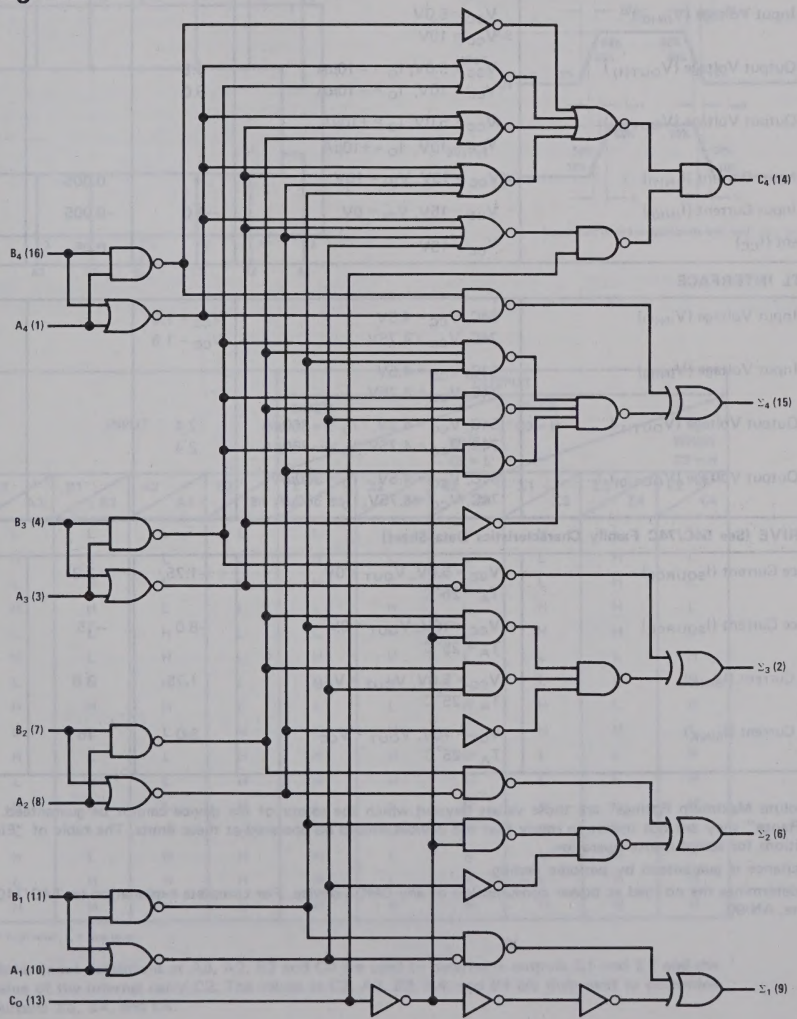
general description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_0) is included and the sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inverison.

features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Fast carry ripple (C_0 to C_4)	50 ns typ @ V_{CC} = 10V and C_L = 50 pF
■ Fast summing (Σ_{IN} to Σ_{OUT})	125 ns typ @ V_{CC} = 10V and C_L = 50 pF

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C83	−55°C to +125°C
MM74C83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

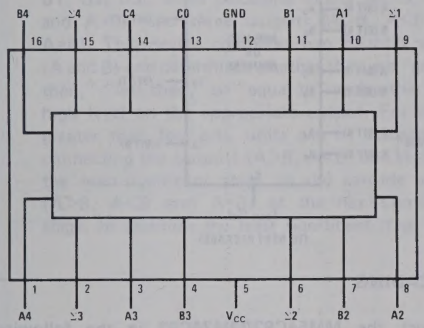
ac electrical characteristics

$T_A = 25^\circ C$, $C_L = 50$ pF, unless otherwise specified.

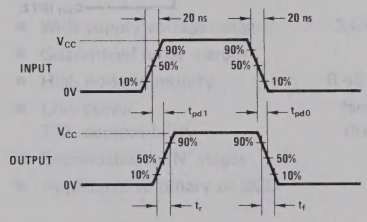
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from C_0 to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		120	200	ns
	$V_{CC} = 10V$		50	80	ns
Propagation Delay from Sum Inputs to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		250	450	ns
	$V_{CC} = 10V$		90	150	ns
Propagation Delay from C_0 to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		350	550	ns
	$V_{CC} = 10V$		125	200	ns
Propagation Delay from Sum Inputs to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		300	550	ns
	$V_{CC} = 10V$		110	180	ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	Per Package (Note 3)		120		pF

connection diagram

Dual-In-Line Package



switching time waveforms



Inputs must be tied to appropriate logic level.

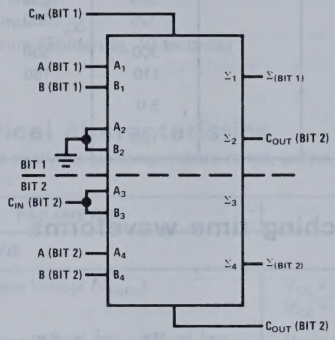
truth table

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

H = high level, L = low level

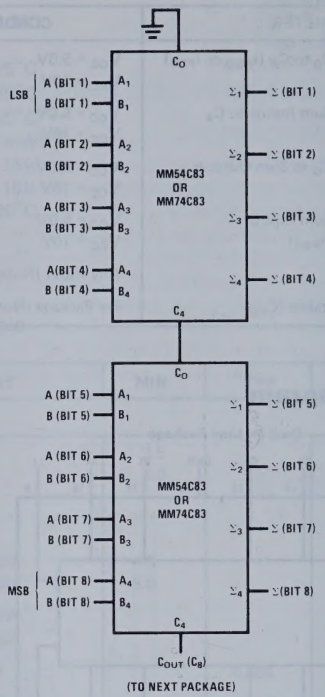
Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

typical applications



APPLICATION

Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.

MM54C85/MM74C85 4-bit magnitude comparator

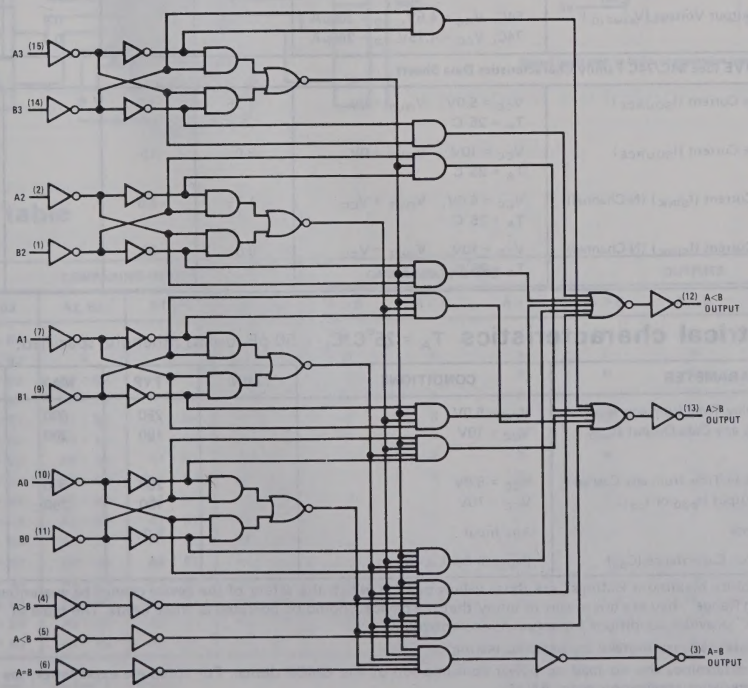
general description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A=B), and three outputs (A>B, A<B and A=B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B, and A=B) of the least-significant stage to the cascade inputs (A>B, A<B and A=B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A=B input and low level voltages ($V_{IN(0)}$) applied to A>B and A<B inputs.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Expandable to 'N' stages
- Applicable to binary or BCD

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C85	−55°C to +125°C
MM74C85	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time from any A or B Data Input to any Data Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V		250	600	ns
	V_{CC} = 10V		100	300	ns
Propagation Delay Time from any Cascade Input to any Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V		200	500	ns
	V_{CC} = 10V		100	250	ns
Input Capacitance	Any Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Package		45		pF

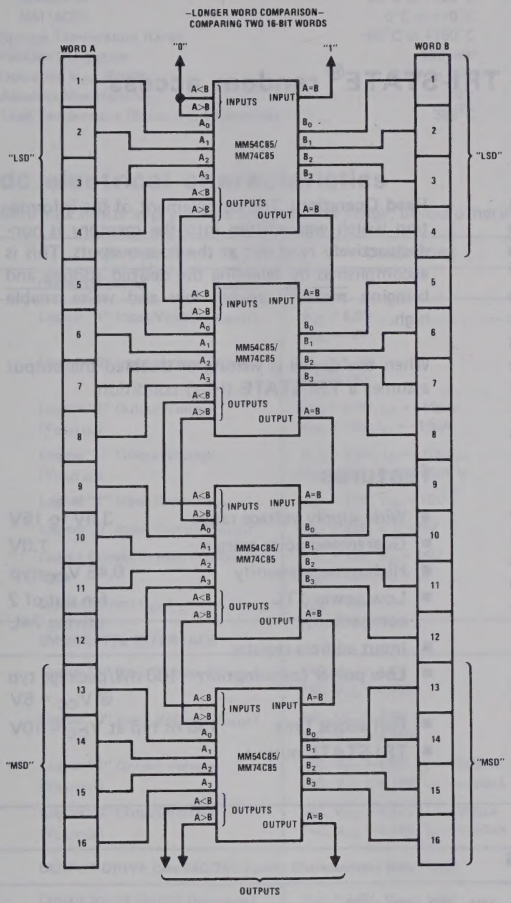
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

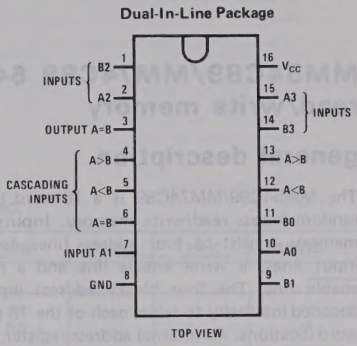
typical application

Four Digit Comparator



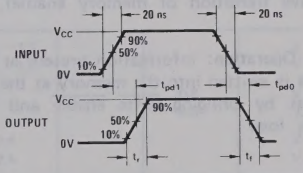
connection diagram

Dual-In-Line Package



TOP VIEW

switching time waveform



Unused inputs must be tied to an appropriate logic level.

truth table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

MM54C89/MM74C89 64-bit TRI-STATE® random access read/write memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

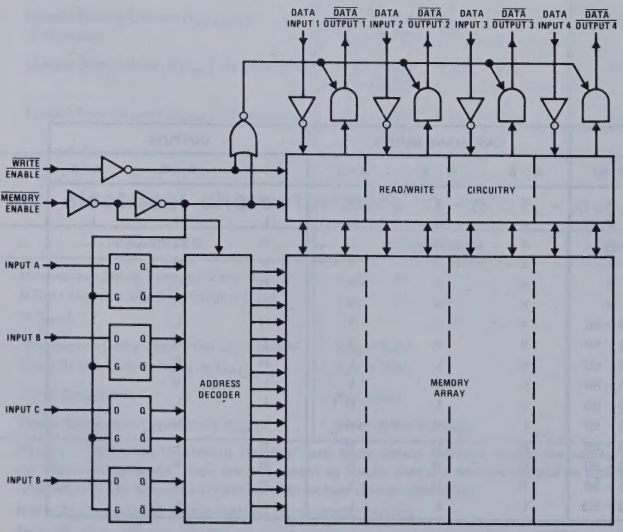
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

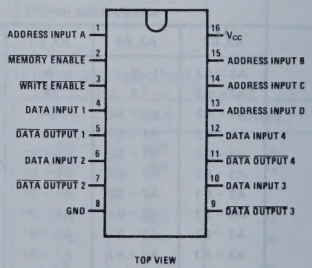
features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V	0			ns
	V_{CC} = 10V	0			ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V			t_{ME}	ns
	V_{CC} = 10V			t_{ME}	ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0	300	160		ns
	V_{CC} = 10V, t_{WS} = 0	100	60		ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

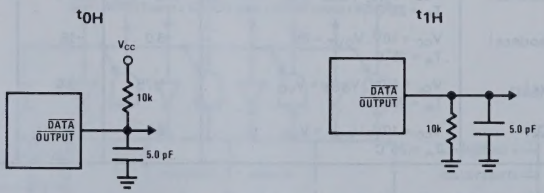
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

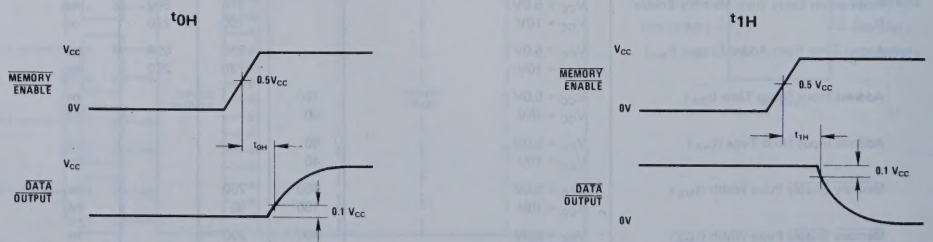
truth table

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

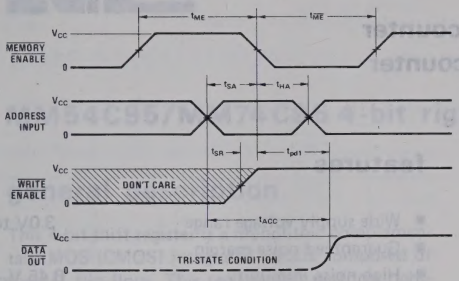


switching time waveforms

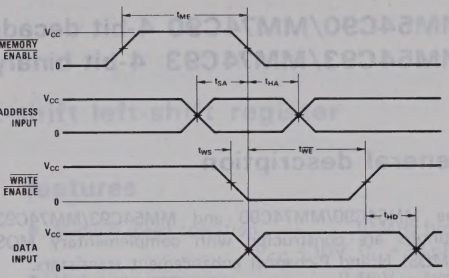


switching time waveforms (con't)

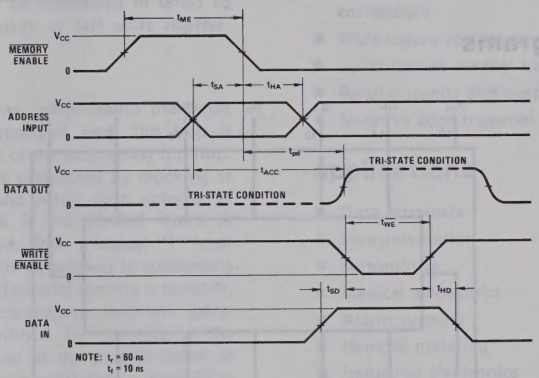
Read Cycle



Write Cycle



Read Modify Write Cycle



Advance Information

MM54C90/MM74C90 4-bit decade counter
MM54C93/MM74C93 4-bit binary counter

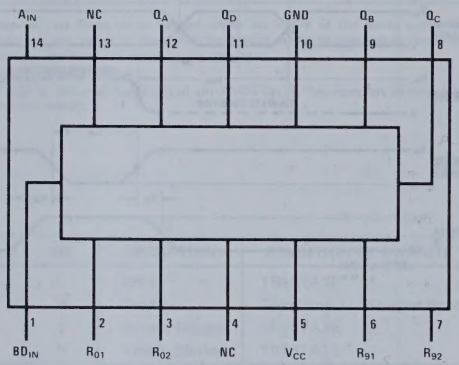
general description

The MM54C90/MM74C90 and MM54C93/MM74C93 counters are constructed with complementary MOS (CMOS) N and P-channel enhancement transistors.

features

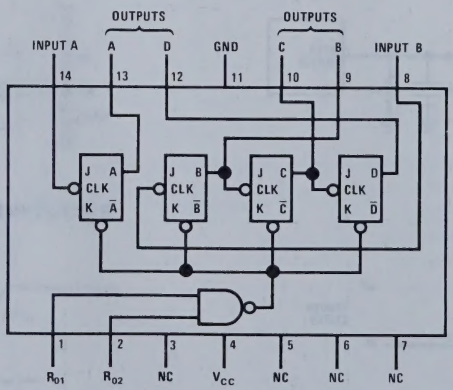
- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Lower power TTL — loads

connection diagrams



TOP VIEW

MM54C90/MM74C90
4-Bit Decade Counter


OUTPUTS
OUTPUTS
INPUT A A D GND C B INPUT B
14 13 12 11 10 9 8
J A CLK K $\bar{A}$
J B CLK K $\bar{B}$
J C CLK K $\bar{C}$
J D CLK K $\bar{D}$
1 2 3 4 5 6 7
R_{01} R_{02} NC V_{CC} NC NC NC

TOP VIEW

MM54C93/MM74C93
4-Bit Binary Counter

MM54C95/MM74C95 4-bit right-shift left-shift register

general description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right shift or left shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

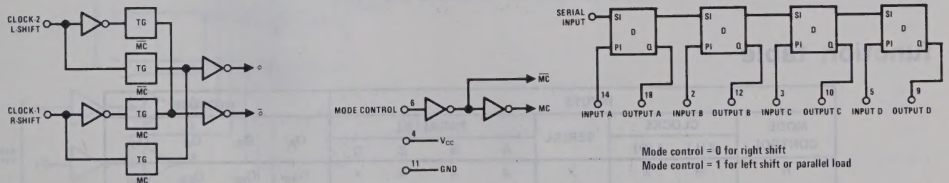
features

- Medium speed operation — 10 MHz typ (V_{CC} = 10V, C_L = 50 pF)
- High noise immunity — 0.45 V_{CC} typ
- Low power — 100 nW typ
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking

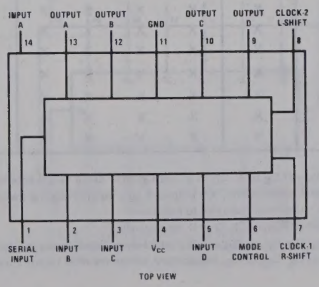
applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

block and connection diagrams



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V	Maximum V_{CC} Voltage	16V
Operating Temperature	MM54C95	−55°C to +125°C	Package Dissipation	500 mW
	MM74C95	0°C to +70°C	Operating V_{CC} Range	+3V to +15V
Storage Temperature		−65°C to +150°C	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

Max/min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	160	ns
Time Prior to Clock Pulse That Data Must be Preset t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		15		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		10		ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		50		ns
Minimum Mode Control Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40		ns
Maximum Input Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	3	4.5		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	6.5	10		MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = −100 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = −100 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		175		ns

Note 1: These devices should not be connected under "Power On" conditions.

function table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL							
	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

MM54C151/MM74C151 8 channel digital multiplexer

general description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the stroke input forces W to a logical "0" and Y to a logical "1".

All inputs are protected against electrostatic effects.

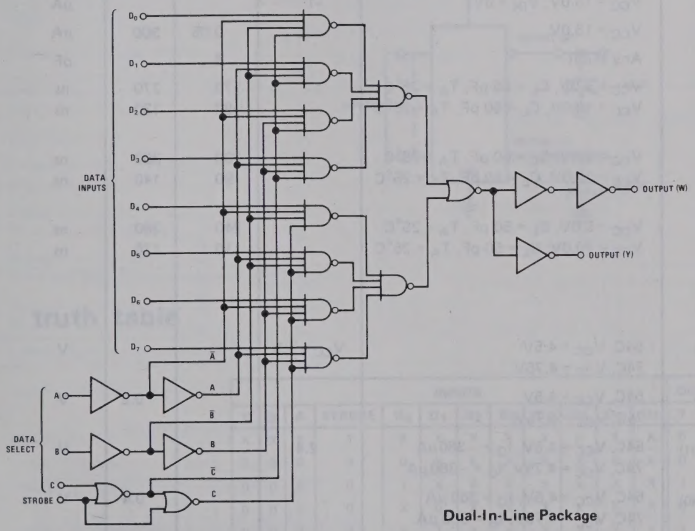
features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} typ
- Low power 50 nW typ

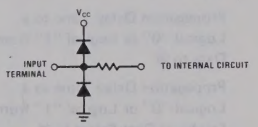
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

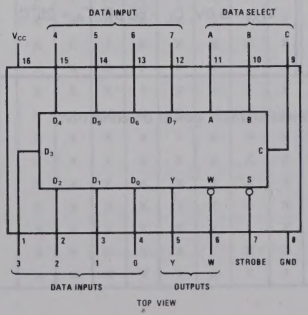
logic and connection diagrams



Input Protection For All Inputs



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C151	−55°C to +125°C
	MM74C151	0°C to +70°C
Storage Temperature		−65°C to +150°C
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

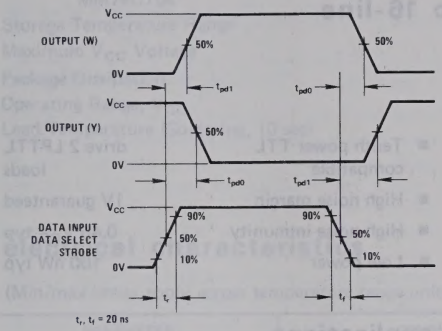
Min/Max limits apply across temperature range across otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10.0V	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10.0V			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
		V_{CC} = 10.0V, I_O = − 10 μA	9			V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 5.0V, I_O = +10 μA			0.5	V
		V_{CC} = 10.0V, I_O = +10 μA			1	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15.0V, V_{IN} = 15V			1	μA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15.0V, V_{IN} = 0V	−1			μA
Supply Current	I_{CC}	V_{CC} = 15.0V		0.05	300	μA
Input Capacitance		Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	270	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	130	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Data to W		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	300	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	140	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	360	ns
		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		110	170	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or a Logical "1" t_{pd1} from Data Input, to Y		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	320	ns

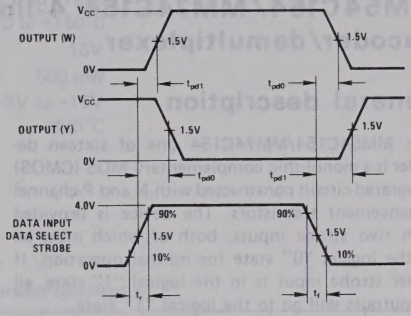
Note 1: This device should not be connected under power on conditions.

switching time waveforms

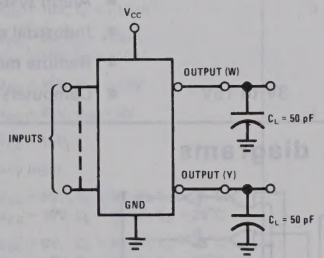
CMOS to CMOS (t_{pd1} & t_{pd0})



TTL to CMOS (t_{pd1} & t_{pd0})



ac test circuit



truth table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

MM54C154/MM74C154 4-line to 16-line decoder/demultiplexer

general description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

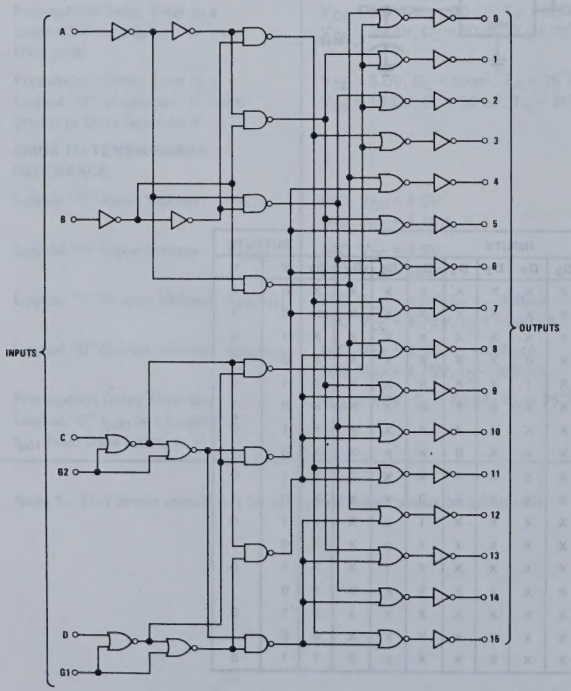
features

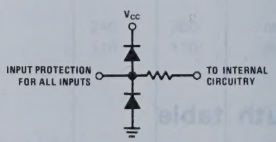
■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise margin	1V guaranteed
■ High noise immunity	0.45 V_{CC} typ
■ Low power	100 nW typ

applications

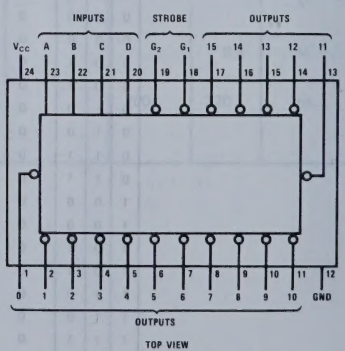
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams





Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C154	−55°C to +125°C
MM74C154	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating Range, V_{CC}	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

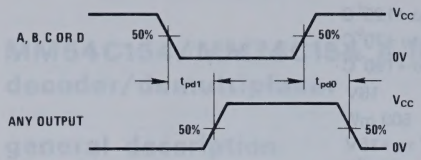
electrical characteristics

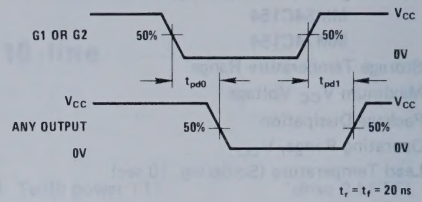
(Min/max limits apply across temperature range unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10 V			1.5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay to a Logical "0" From Any Input to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "0" From G1 or G2 to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "1" From Any Input to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
Propagation Delay to a Logical "1" From G1 or G2 to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4.5V, I_O = −100μA 74C V_{CC} = 4.75V, I_O = −100μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4	V

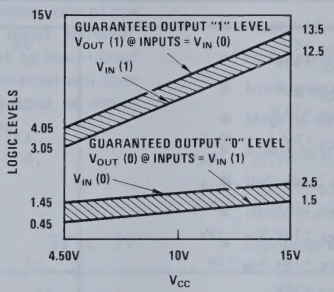
Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

switching time waveforms





Guaranteed Noise Margin as a Function of V_{CC}



truth table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

MM54C157/MM74C157 quad 2-input multiplexers

general description

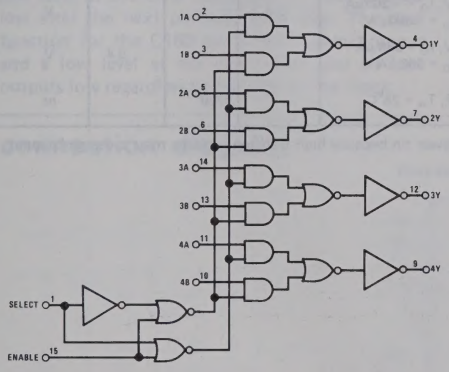
These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1" the outputs assume logical "0." Select decoding is done internally resulting in a single select input only.

- Low power — 50 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads

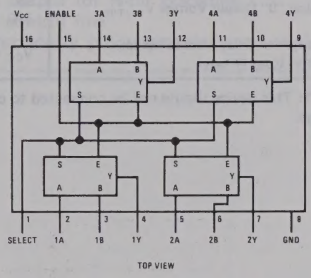
features

- Supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ

schematic and connection diagrams



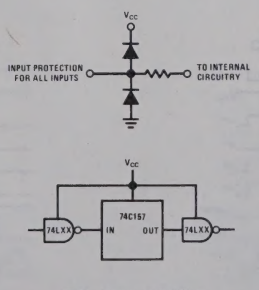
Dual-In-Line Package



TOP VIEW

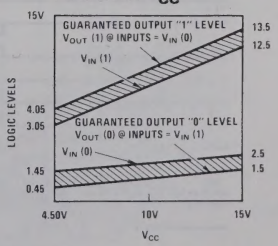
truth table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1



74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} to 0.3V	Storage Temperature	−65°C to 150°C
Operating Temperature	MM54C157	−55°C to 125°C	Package Dissipation	500 nW
	MM74C157	0°C to 70°C	Lead Temperature (Soldering, 10 sec)	300°C
Maximum V_{CC} Voltage		16V	Operating V_{CC} Range	+3V to 15V

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	15	μA
Input Capacitance	Any Input		5		pF
Propagation Delay from Data to Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		150	250	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		80	130	ns
Propagation Delay from Enable to Output (t_{pd0})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		80	130	ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4.5V				
	74C V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4.5V				
	74C V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4.5V, I_O = −360μA				
	74C V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, I_O = 360 μA				
	74C V_{CC} = 4.75V, I_O = 360 μA			0.4	V
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		250		ns

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

MM54C160/MM74C160 decade counter with asynchronous clear
MM54C161/MM74C161 binary counter with asynchronous clear
MM54C162/MM74C162 decade counter with synchronous clear
MM54C163/MM74C163 binary counter with synchronous clear

general description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

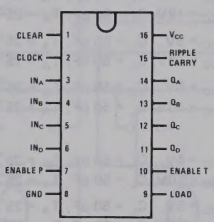
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

features

- High noise margin — 1V guaranteed
- High noise immunity — 0.45 V_{CC} typ
- Tenth power TTL compatible — drives 2 LPTTL loads
- Wide supply voltage range — 3V to 15V
- Internal look-ahead for fast counting scemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

connection diagram

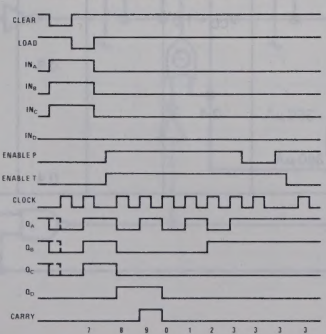
Dual-In-Line Package



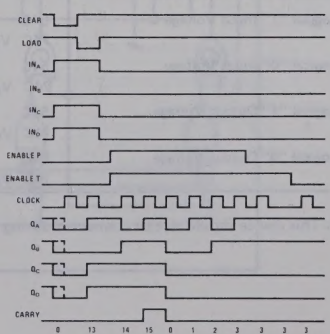
TOP VIEW

logic waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters



absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

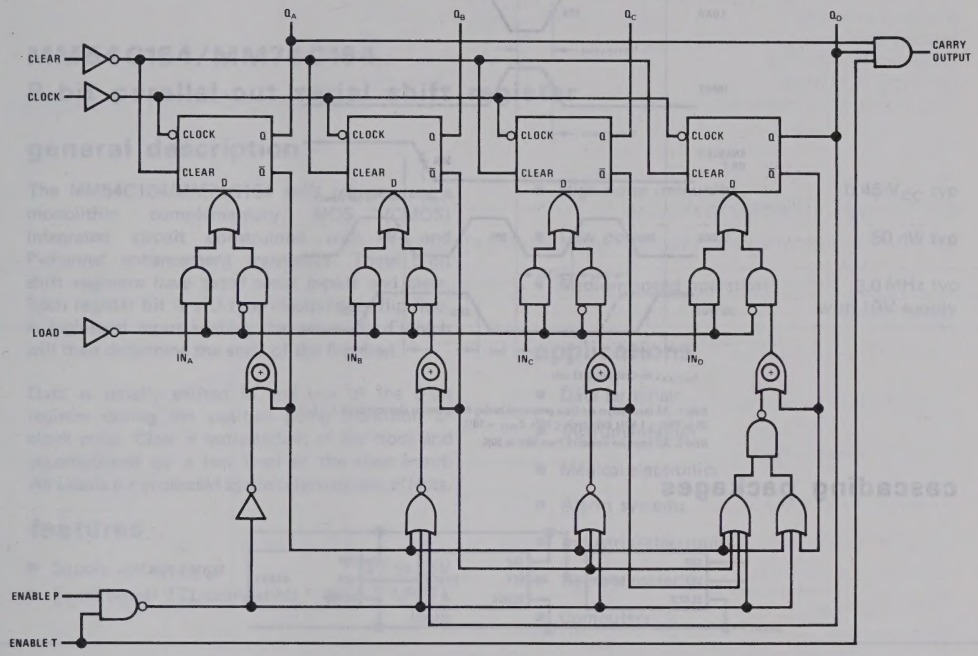
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS to CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5V, I_O = −10 μA	4.5			V
	V_{CC} = 10V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5V, I_O = +10 μA			0.5	V
	V_{CC} = 10V, I_O = +10 μA			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation delay time from clock to Q t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100	160	ns
Propagation delay time from clock to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		290	450	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120	190	ns
Propagation delay time from T enable to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		180	290	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70		ns
Propagation time from clear to Q (C162 and C163 only) t_{pd0}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		190	300	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		80		ns
Time prior to clock that data or load must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		30		ns
Time prior to clock that enable P or T must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		170	280	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70	120	ns
Time prior to clock that clear must be present (162, 163 only) t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120	190	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		50	80	ns
Minimum clock pulses width t_{WL} or t_{WH}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		90	170	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		35	70	ns
Maximum clock rise or fall time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C			15	μs
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			5.0	μs
Maximum clock frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C	5.5	8.5		MHz
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage	54C V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA	2.4			V
	74C V_{CC} = 4.75V				
Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA				V
	74C V_{CC} = 4.75V			0.4	

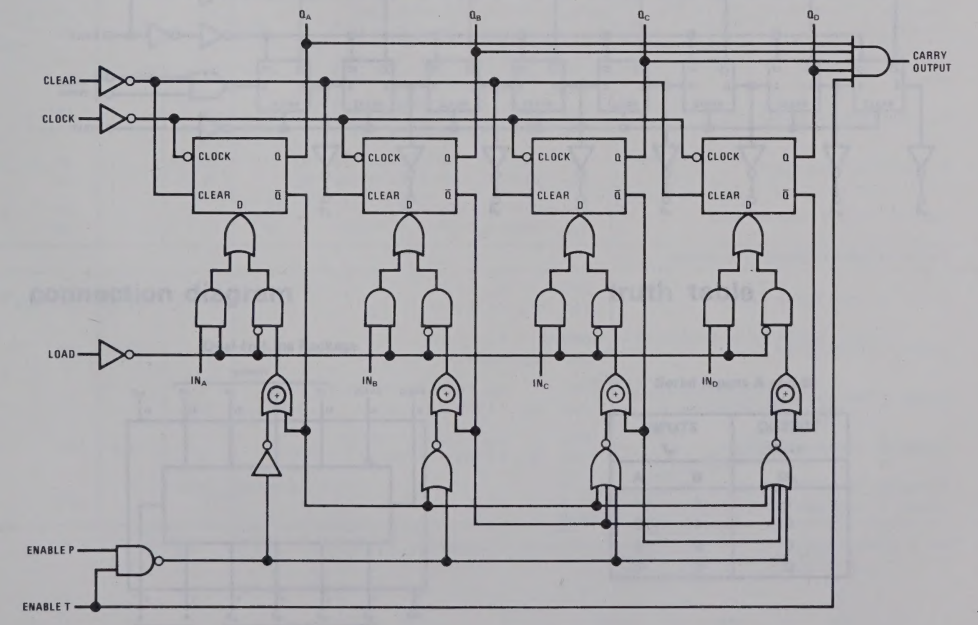
Note 1: This device should not be connected during power on conditions.

logic diagrams

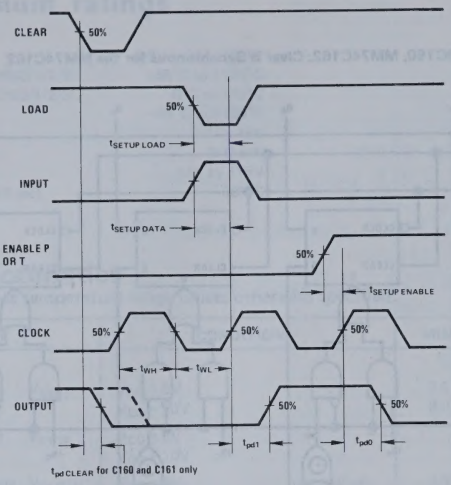
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



MM74C161, MM74C163; Clear is Synchronous for the MM74C163



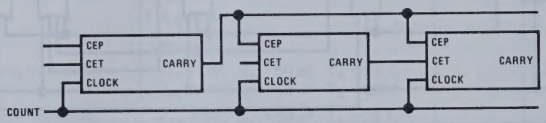
switching time waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f =$ 20 ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

cascading packages



MM54C164/MM74C164
8-bit parallel-out serial shift register

general description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

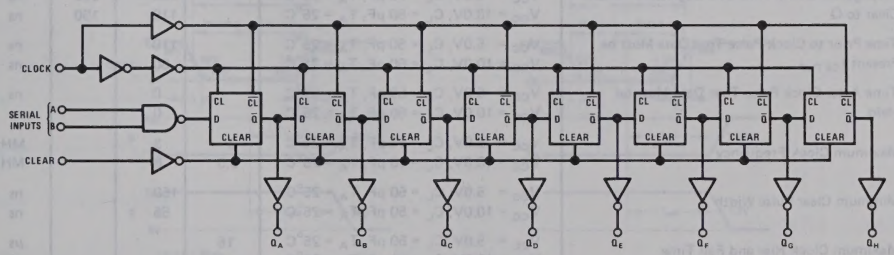
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} typ
- Low power — 50 nW typ
- Medium speed operation — 8.0 MHz typ with 10V supply

applications

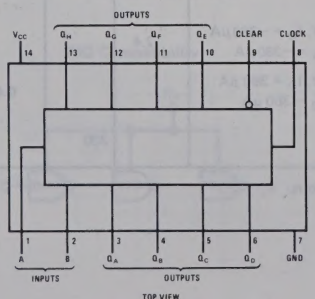
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote meterly
- Computers

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

Serial Inputs A and B

INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C164	$-55^{\circ}C$ to $+125^{\circ}C$
	MM74C164	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature		$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation		500 mW
Maximum V_{CC} Voltage		16V
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		$300^{\circ}C$

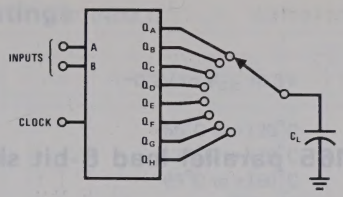
electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

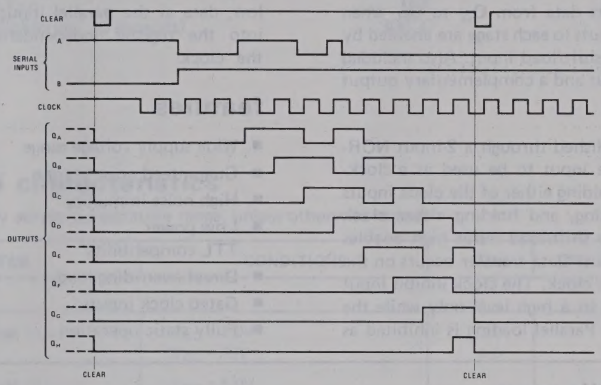
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V $I_O = -10\,\mu A$	4.5			V
	V_{CC} = 10.0V $I_O = -10\,\mu A$	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V $I_O = -10\,\mu A$			0.5	V
	V_{CC} = 10.0V $I_O = -10\,\mu A$			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V V_{IN} = 0V	−1	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" From Clock to Q	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		230	310	ns
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		90	120	ns
Propagation Delay Time to a Logical "1" From Clear to Q	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		280	380	ns
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		110	150	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		110		ns
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		30		ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		0		ns
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$	2	3		MHz
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$	5.5	8		MHz
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$		55		ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, $T_A = 25^{\circ}C$	15			μs
	V_{CC} = 10.0V, C_L = 50 pF, $T_A = 25^{\circ}C$	5			μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4.5V	$V_{CC}-1.5$			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4.5V, $I_O = -360\,\mu A$	2.4			V
	74C V_{CC} = 4.75V, $I_O = -360\,\mu A$				
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, $I_O = 360\,\mu A$			0.4	V
	74C V_{CC} = 4.75V, $I_O = 360\,\mu A$				
Propagation Delay Time to a Logical "0" or Logical "1" From Clock To Q			320		ns

Note 1: These devices should not be connected under power on conditions.

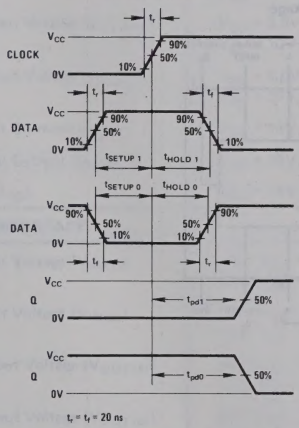
ac test circuit



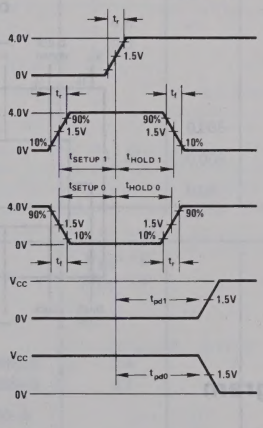
switching time waveforms



CMOS to CMOS

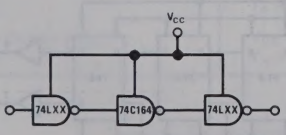


TTL to CMOS

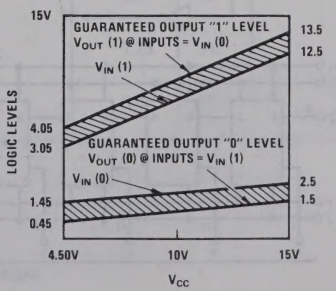


typical applications

74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



MM54C165/MM74C165 parallel-load 8-bit shift register

general description

The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth-bit.

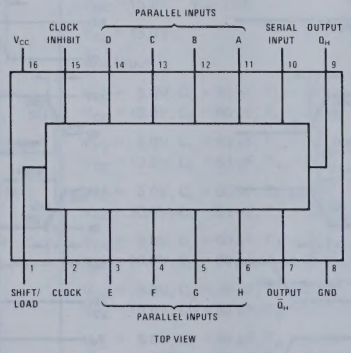
Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load input high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Direct overriding load
- Gated clock inputs
- Fully static operation

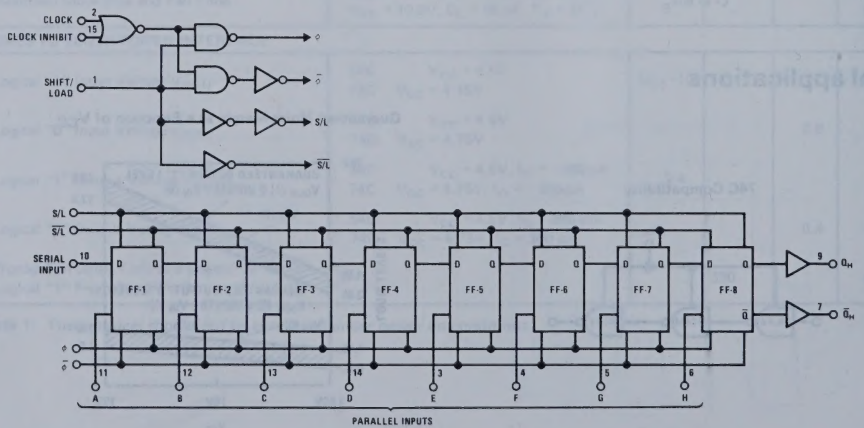
connection diagram

Dual-In-Line Package



TOP VIEW

block diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C165	−55°C to +125°C
MM74C165	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

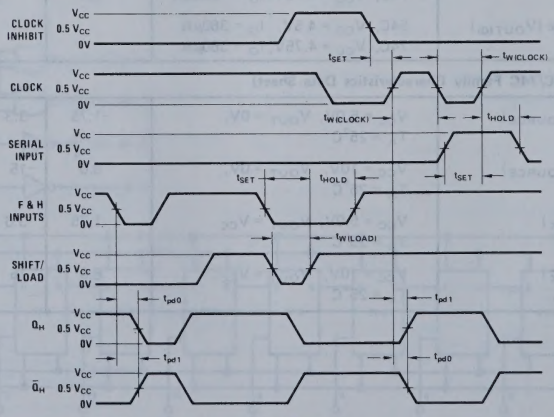
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from Clock or Load to Q or $\overline{Q}$	V_{CC} = 5.0V		200	400	ns
	V_{CC} = 10V		80	200	ns
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from H to Q or $\overline{Q}$	V_{CC} = 5.0V		200	400	ns
	V_{CC} = 10V		80	200	ns
Clock Inhibit Set-up Time	V_{CC} = 5.0V	150	75		ns
	V_{CC} = 10V	60	30		ns
Serial Input Set-up Time	V_{CC} = 5.0V	50	25		ns
	V_{CC} = 10V	30	15		ns
Serial Input Hold Time	V_{CC} = 5.0V	50	0		ns
	V_{CC} = 10V	30	0		ns
Parallel Input Set-up Time	V_{CC} = 5.0V	150	75		ns
	V_{CC} = 10V	60	30		ns
Parallel Input Hold Time	V_{CC} = 5.0V	50	0		ns
	V_{CC} = 10V	30	0		ns
Minimum Clock Pulse Width	V_{CC} = 5.0V		70	200	ns
	V_{CC} = 10V		30	100	ns
Minimum Load Pulse Width	V_{CC} = 5.0V		85	180	ns
	V_{CC} = 10V		30	90	ns
Maximum Clock Frequency	V_{CC} = 5.0V		6.0	2.5	MHz
	V_{CC} = 10V		12	5.0	MHz
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	10			μs
	V_{CC} = 10V	5.0			μs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms



Note A: The remaining six data and the serial input are low.

Note B: Prior to test, high level data is loaded into H input.

truth table

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$

X = irrelevant

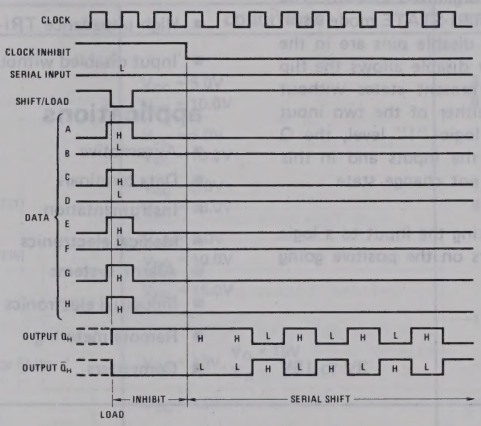
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$

a . . . h = the level at data inputs A thru H

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock

logic waveforms



MM54C173/MM74C173 TRI-STATE® quad D flip–flop

general description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The four D type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive going transition.

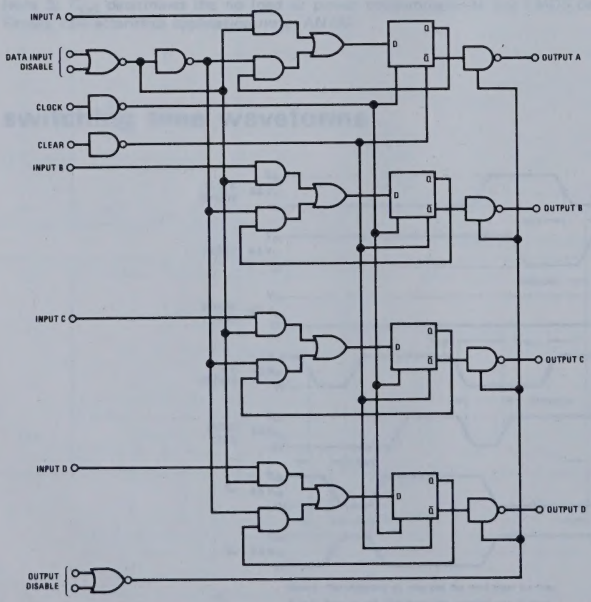
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — Drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} typ
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disabled without gating the clock

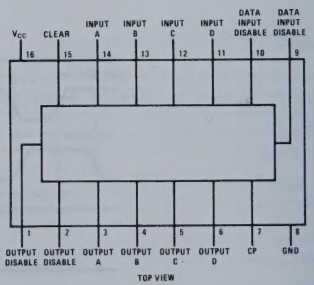
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3 to V_{CC} +0.3V
Operating Temperature	MM54C173	−55°C to +125°C
	MM74C173	0°C to +70°C
Storage Temperature		−65°C to +150°C
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Operating V_{CC} Range		+3V to +15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V		0.005	1	μA
Logical "0" Input Current $I_{IN(0)}$		−1	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.001		μA
	V_{CC} = 15V, V_O = 0V		0.001		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		220	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	200	ns
Input Data Setup Time, $t_{S\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		40	80	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15	30	ns
Input Data Hold Time, $t_{H\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Input Disable Setup Time, $t_{S\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		35	70	ns
Input Disable Hold Time, $t_{H\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Delay From Output Disable to High Impedance State (From Logical "1" or Logical "0" Level), t_{1H}, t_{0H}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "1" Level, t_{H1} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "0" Level, t_{HO} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Propagation Delay From Clear to Output t_{pdR}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	490	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	180	
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	3.0	4.0		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	7	12		
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70		
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	10			μs
	V_{CC} = 10.0V, C_L = 50 pF	5			μs

Note 1: These devices should not be connected under "Power On" conditions.

electrical characteristics (con't)

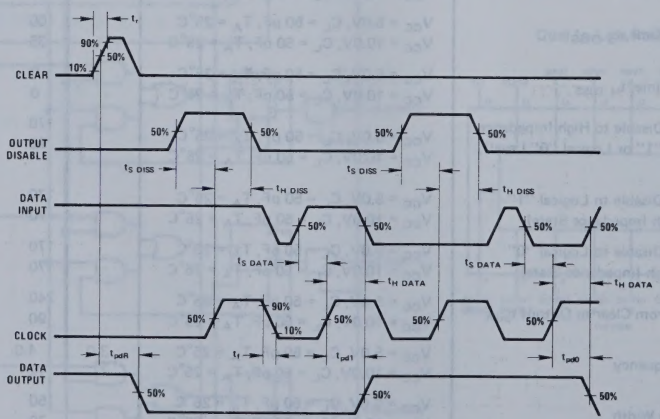
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	$V_{CC}-1.5$			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			.4	V
Propagation Delay Time to a Logical "0", t_{pd0} or Logical "1" t_{pd1} From Clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		500		ns

truth table

Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

switching time waveforms



MM54C174/MM74C174 hex D flip-flop

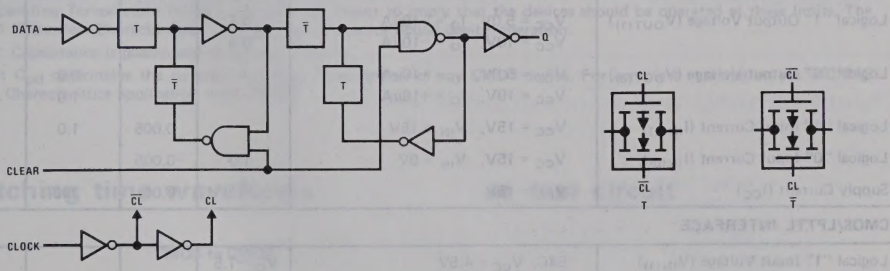
general description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{CC} and GND.

features

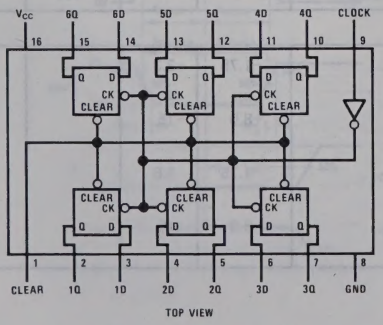
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C174	−55°C to +125°C
MM74C174	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q	V_{CC} = 5.0V		150	300	ns
	V_{CC} = 10V		70	110	ns
Propagation Delay Time to a Logical "0" from Clear	V_{CC} = 5.0V		110	300	ns
	V_{CC} = 10V		50	110	ns
Time Prior to Clock Pulse that Data Must be Present (t_{SETUP})	V_{CC} = 5.0V	75			ns
	V_{CC} = 10V	25			ns
Time After Clock Pulse that Data Must be Held (t_{HOLD})	V_{CC} = 5.0V	75			ns
	V_{CC} = 10V	25			ns
Minimum Clock Pulse Width	V_{CC} = 5.0V		50		ns
	V_{CC} = 10V		35		ns
Minimum Clear Pulse Width	V_{CC} = 5.0V		65	140	ns
	V_{CC} = 10V		35	70	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	15	>1200		μs
	V_{CC} = 10V	5.0	>1200		μs
Maximum Clock Frequency	V_{CC} = 5.0V	2.0	6.5		MHz
	V_{CC} = 10V	5.0	12		MHz
Input Capacitance (C_{IN})	Clear Input (Note 2)		11		pF
	Any Other Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		95		pF

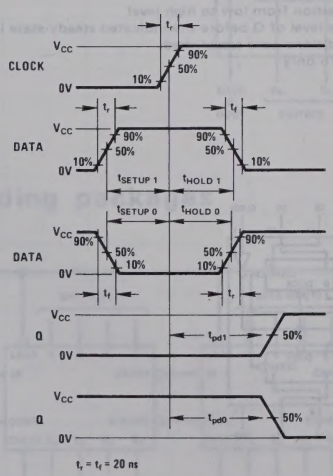
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

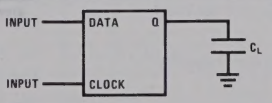
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

CMOS to CMOS



ac test circuit



Advance Information

MM54C175/MM74C175 quad D flip-flop

general description

These monolithic positive-edge-triggered flip-flops utilize complementary MOS (CMOS) integrated circuitry to implement D-type flip-flop logic. Both have a direct clear input and the 'C175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

features

- Wide supply voltage range — 3.0 V to 15 V
- Guaranteed noise margin — 1.0 V
- High noise immunity — 0.45 V_{CC} typ
- Low power T^2L compatible — drive 2 LT^2L loads

application

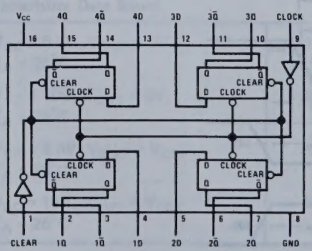
- Automotive
- Instrumentation
- Alarm systems
- Remote metering
- Data terminals
- Medical electronics
- Industrial controls
- Computers

function table and connection diagram

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = 'C175 only



MM54C175/MM74C175
Quad D Flip-Flop

MM54C192/MM74C192 synchronous 4-bit up/down decade counter
MM54C193/MM74C193 synchronous 4-bit up/down binary counter

general description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters. While the MM54C193 and MM74C193 are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

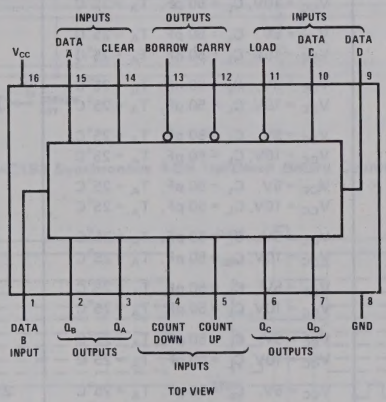
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1." The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

features

- High noise margin — 1V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} typ

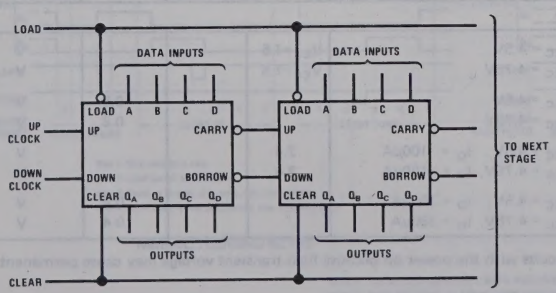
connection diagram

Dual-In-Line Package

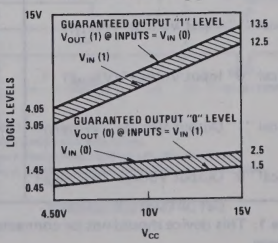


TOP VIEW

cascading packages



Guaranteed Noise Margin as A Function of V_{CC}



absolute maximum ratings

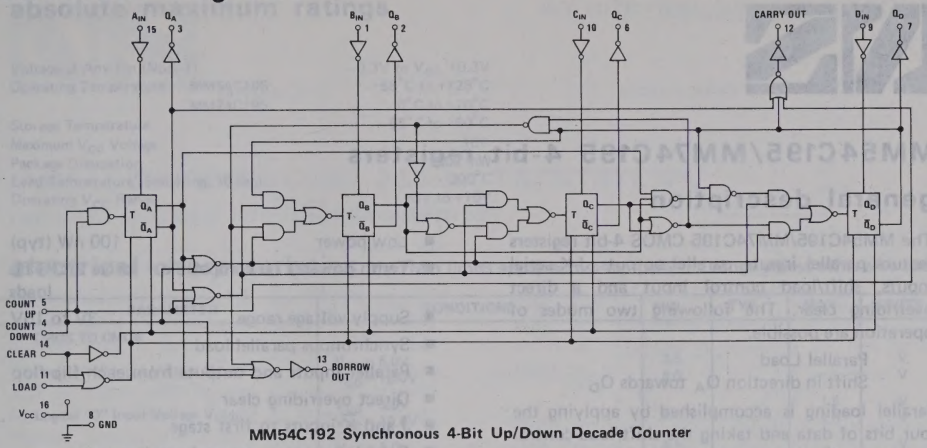
Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C192, MM54C193	−55°C to +125°C
MM74C192, MM74C193	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Min/max limits apply across temperature range unless otherwise specified.)

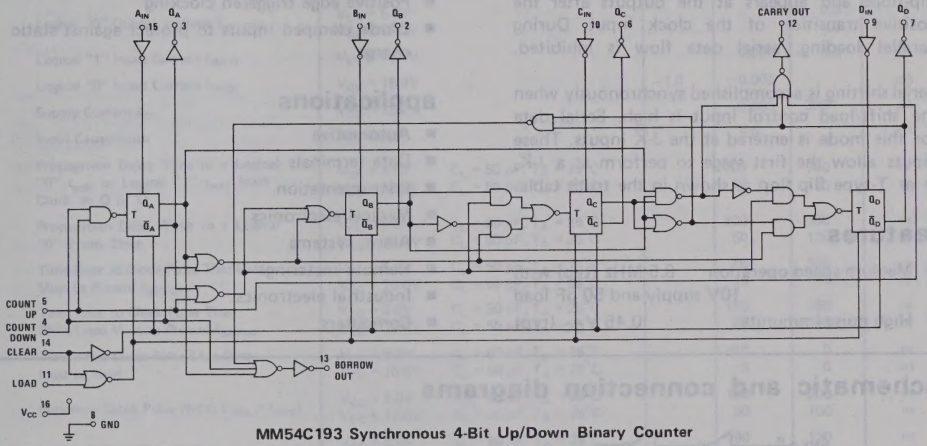
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO MOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to Q From Count Up or Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100	160	ns
Propagation Delay Time to Borrow From Count Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120	200	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		50	80	ns
Propagation Delay Time to Carry From Count Up (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120	200	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		50	80	ns
Time Prior to Load That Data Must be Present (t_{SETUP})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		100	160	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		30	50	ns
Minimum Clear Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		300	480	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120	190	ns
Minimum Load Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		100	160	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		40	65	ns
Propagation Delay Time to Q From Load (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		300	480	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120	190	ns
Minimum Count Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120	200	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		35	80	ns
Maximum Count Frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	2.5	4		MHz
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C	6	10		MHz
Count Rise and Fall Time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C			15	μs
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			5	μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4.5V	V_{CC}−1.5			V
	74C V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4.5V, I_O = −100μA	2.4			V
	74C V_{CC} = 4.75V, I_O = −100μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C V_{CC} = 4.75V, I_O = 360μA			0.4	V

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

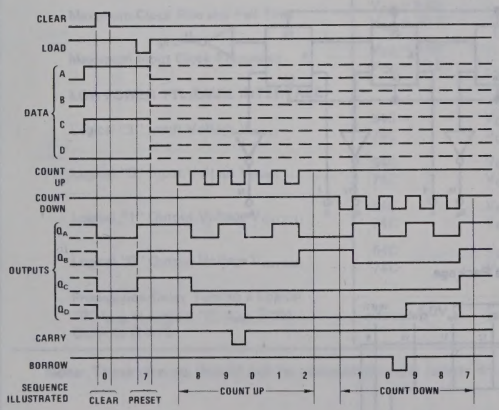
schematic diagrams



MM54C192 Synchronous 4-Bit Up/Down Decade Counter

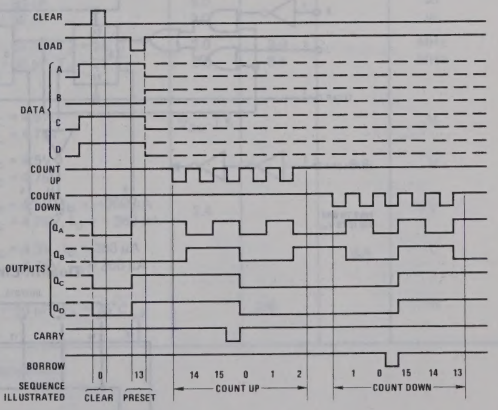


MM54C193 Synchronous 4-Bit Up/Down Binary Counter



Note 1: Clear outputs to zero.
Note 2: Load (preset) to BCD seven.
Note 3: Count up to eight, nine, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, nine, eight, and seven.

MM54C192/MM74C192



Note 1: Clear outputs to zero.
Note 2: Load (preset) to binary thirteen.
Note 3: Count up to fourteen, fifteen, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM54C193/MM74C193

NOTE A: CLEAR OVERRIDES LOAD, DATA, AND COUNT INPUTS.
NOTE B: WHEN COUNTING UP, COUNT DOWN INPUT MUST BE HIGH; WHEN COUNTING DOWN, COUNT-UP INPUT MUST BE HIGH.

MM54C195/MM74C195 4-bit registers

general description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible.

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip flop as shown in the truth table.

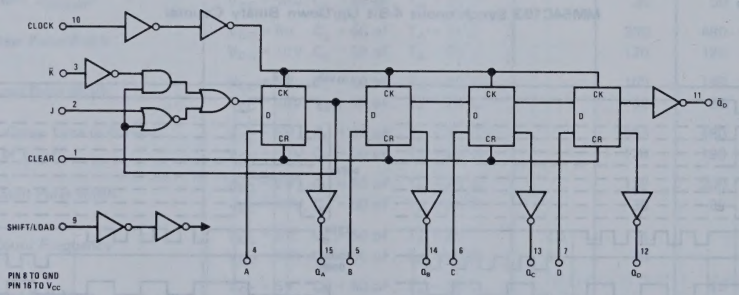
features

- Medium speed operation — 8.5 MHz (typ) with 10V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — 100 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads
- Supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- Positive edge triggered clocking
- Diode clamped inputs to protect against static charge

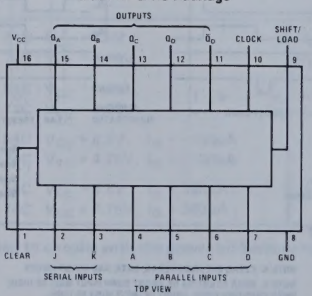
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

schematic and connection diagrams



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C195	−55°C to +125°C
	MM74C195	0°C to +70°C
Storage Temperature		−65°C to 150°C
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Lead Temperature (Soldering, 10 sec)		300°C
Operating V_{CC} Range		+3V to +15V

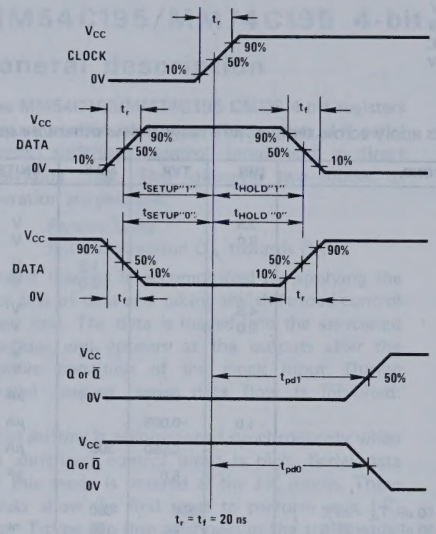
electrical characteristics Max/Min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V		3.5			V
	V_{CC} = 10.0V		8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V				1.5	V
	V_{CC} = 10.0V				2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V		4.5			V
	V_{CC} = 10.0V		9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V				0.5	V
	V_{CC} = 10.0V				1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V		−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0V			0.050	300	μA
Input Capacitance	Any Input			5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		200	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		75	130	ns
Propagation Delay Time to a Logical "0" From Clear	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		100	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	130	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		60	100	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		15	50	ns
Time Prior to Clock Pulse That Shift/Load Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		110	150	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		60	90	ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		−10	0	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		−5	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	100	ns
Minimum Clear Pulse Width	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		90	130	ns
	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		40	60	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	C_L = 50 pF	5.0			μs
	V_{CC} = 10.0V	C_L = 50 pF	2.0			μs
Maximum Input Clock Frequency	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C	5.5	8.5		MHz
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage $V_{IN(1)}$	54C	V_{CC} = 4.5V	V_{CC}-1.5			V
	74C	V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C	V_{CC} = 4.5V			0.8	V
	74C	V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	V_{CC} = 4.5V, I_D = −360 μA	2.4			V
	74C	V_{CC} = 4.75V, I_D = −360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	V_{CC} = 4.5V, I_D = 360 μA			0.4	V
	74C	V_{CC} = 4.75V, I_D = 360 μA				
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		250		ns

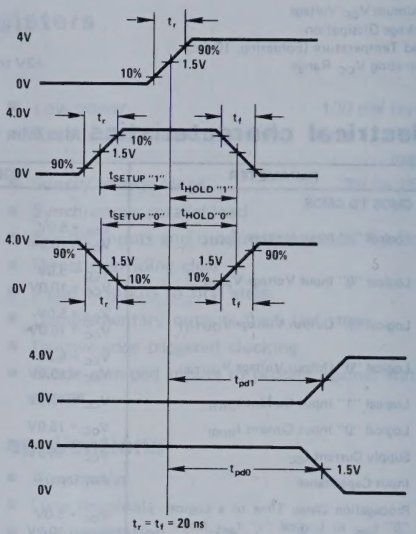
Note: These devices should not be connected under power on condition.

switching time waveforms

CMOS to CMOS



TTL to CMOS

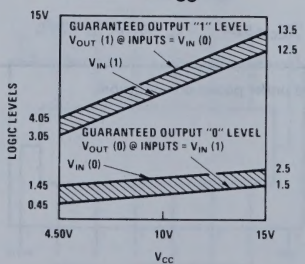


truth table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



Advance Information

MM54C200/MM74C200 256-bit TRI-STATE® random access read/write memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

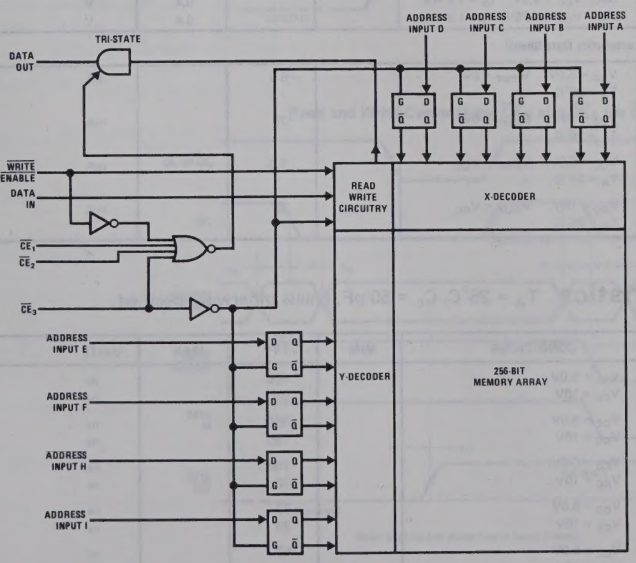
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

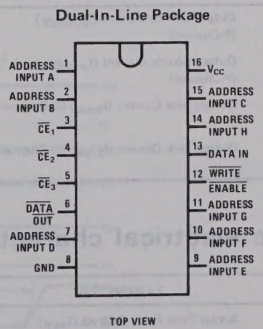
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatibility — fan out of 1 driving standard TTL
- Low power — 500 nW typ
- Internal address register

logic and connection diagrams





absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C		−6.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C		−25		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C		8.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C		30		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V		400		ns
	V_{CC} = 10V		160		ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V		350		ns
	V_{CC} = 10V		140		ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}}$)	V_{CC} = 5.0V		150		ns
	V_{CC} = 10V		70		ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V		50		ns
	V_{CC} = 10V		20		ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V		60		ns
	V_{CC} = 10V		30		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V V_{CC} = 10V		200 80		ns ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V V_{CC} = 10V		200 80		ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		300		pF

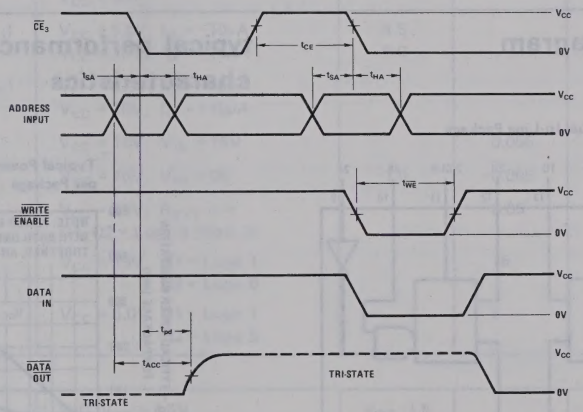
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

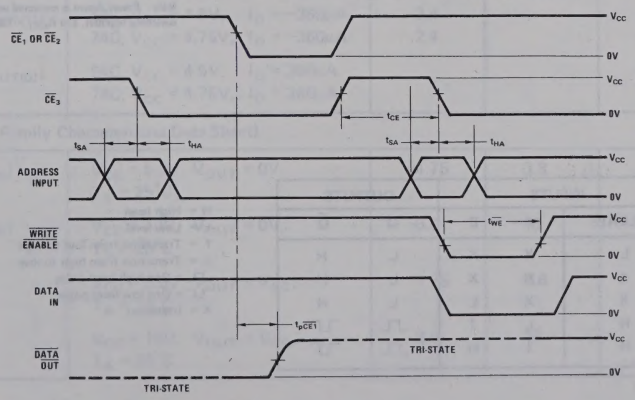
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

Advance Information

MM54C221/MM74C221 dual monostable multivibrators

general description

The MM54C221/MM74C221 dual monostable multivibrators is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

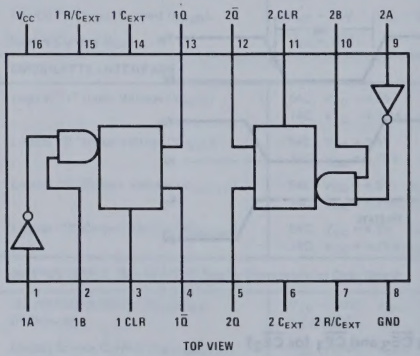
Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}. Pulse stability will be limited by the accuracy of external timing components. The R_{EXT} ranges from 10k to 100k. Throughout these ranges the pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT}\ R_{EXT}$.

features

■ Wide supply voltage range	4.5V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagram

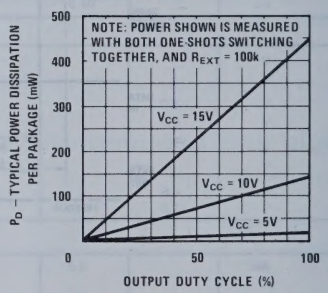
Dual-In-Line Package



TOP VIEW

typical performance characteristics

Typical Power Dissipation per Package



Note: Power shown is measured with both one-shots switching together, and R_{EXT} = 100k.

truth table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎎ = One low level pulse
X = Irrelevant

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C221	−55°C to +125°C
MM74C221	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	4.5V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, R_{EXT} = ∞ Q1, Q2 = Logic 0 (Note 3)		0.05	300	μA
	V_{CC} = 15V, Q1 = Logic 1 Q2 = Logic 0		15		mA
	V_{CC} = 5.0V, Q1 = Logic 1 Q2 = Logic 0		2		mA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

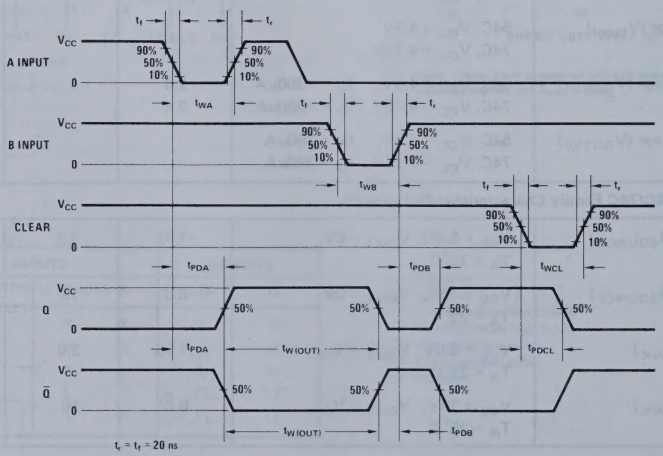
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Trigger Input (A, B) to Output Q, $\overline{Q}$ ($t_{PDA,B}$)	V_{CC} = 5.0V		250	500	ns
	V_{CC} = 10V		120	250	ns
Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$ (t_{PDCL})	V_{CC} = 5.0V		250	500	ns
	V_{CC} = 10V		120	250	ns
Minimum Trigger Input (A, B) Pulse Width ($t_{W(A,B)}$)	V_{CC} = 5.0V	150	65		ns
	V_{CC} = 10V	70	30		ns
Minimum Clear Input (CL) Pulse Width ($t_{W(CL)}$)	V_{CC} = 5.0V	150	65		ns
	V_{CC} = 10V	70	30		ns
Q or $\overline{Q}$ Output Pulse Width ($t_{W(OUT)}$)	V_{CC} = 5.0V R = 10k,	250			ns
	V_{CC} = 10V C = 0 pF,	250			ns
	V_{CC} = 15V	250			ns
	V_{CC} = 5.0V R = 10k,	9.3		12.3	μs
	V_{CC} = 10V C = 1000 pF,	9		11	μs
	V_{CC} = 15V	8.5		10.5	μs
	V_{CC} = 5.0V R = 10k,	900		1200	μs
	V_{CC} = 10V C = 0.1μF,	900		1100	μs
	V_{CC} = 15V	900		1100	μs
Output Duty Cycle	R = 10k, C = 1000 pF			90	%
	R = 10k, C = 0.1μF			95	%
Input Capacitance (C_{IN})	R/C_{EXT} Input		25		pF
	Any Other Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: In standby (Q = Logic 0) the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

switching time waveforms



MM54C901/MM74C901 hex inverting TTL buffer
MM54C902/MM74C902 hex non-inverting TTL buffer
MM54C903/MM74C903 hex inverting PMOS buffer
MM54C904/MM74C904 hex non-inverting PMOS buffer

general description

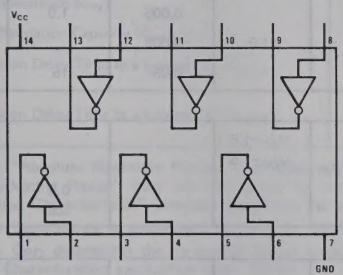
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply. For specific applications see MOS Brief 18 in the back of this catalog.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatibility — fan out of 2 driving standard TTL

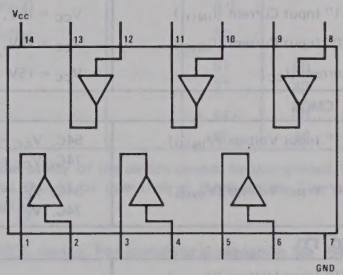
connection and logic diagrams

Dual-In-Line Package
MM54C901/MM74C901
MM54C903/MM74C903



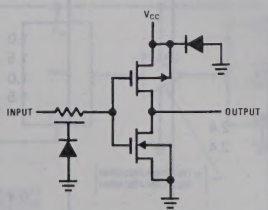
TOP VIEW

Dual-In-Line Package
MM54C902/MM74C902
MM54C904/MM74C904

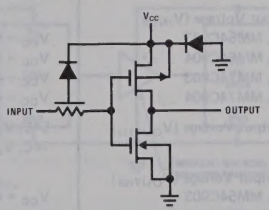


TOP VIEW

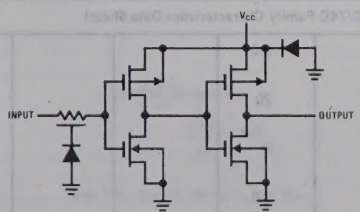
MM54C901/MM74C901
CMOS to TTL Inverting Buffer



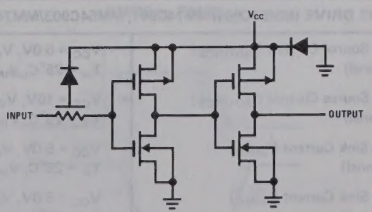
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



MM54C902/MM74C902
CMOS to TTL Buffer



MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



absolute maximum ratings (Note 1)

Voltage at Any Output Pin	$-0.3V$ to V_{CC} $+0.3V$
Voltage at Any Input Pin	
MM54C901/MM74C901	$-0.3V$ to $+15V$
MM54C902/MM74C902	$-0.3V$ to $+15V$
MM54C903/MM74C903	V_{CC} $-17V$ to V_{CC} $+0.3V$
MM54C904/MM74C904	V_{CC} $-17V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C901, MM54C902, MM54C903, MM54C904	$-55^{\circ}C$ to $+125^{\circ}C$
MM74C901, MM74C902, MM74C903, MM74C904	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	15	μA
TTL TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$	$V_{CC}-1.5$			V
	74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$			0.8	V
	74C, $V_{CC} = 4.75V$			0.8	V
CMOS TO TTL					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$	4.0			V
MM54C902, MM54C904	$V_{CC} = 4.5V$	$V_{CC}-1.5$			V
MM74C901, MM74C903	$V_{CC} = 4.75$	4.25			V
MM74C902, MM74C904	$V_{CC} = 4.75$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$			1.0	V
MM54C902, MM54C904	$V_{CC} = 4.5V$			1.5	V
MM74C901, MM74C903	$V_{CC} = 4.75$			1.0	V
MM74C902, MM74C904	$V_{CC} = 4.75$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -800\mu A$	2.4			V
	74C, $V_{CC} = 4.75V$, $I_O = -800\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$, $I_O = 2.6$ mA			0.4	V
MM54C902, MM54C904	$V_{CC} = 4.5V$, $I_O = 3.2$ mA			0.4	V
MM74C901, MM74C903	$V_{CC} = 4.75V$, $I_O = 2.6$ mA			0.4	V
MM74C902, MM74C904	$V_{CC} = 4.75V$, $I_O = 3.2$ mA			0.4	V
OUTPUT DRIVE (MM54C901/MM74C901, MM54C903/MM74C903) (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$, $T_A = 25^{\circ}C$, $V_{IN} = 0V$	5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25^{\circ}C$, $V_{IN} = 0V$	20			mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$, $T_A = 25^{\circ}C$, $V_{IN} = V_{CC}$	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$, $T_A = 25^{\circ}C$, $V_{IN} = V_{CC}$	3.8			mA

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (MM54C902/MM74C902, MM54C904/MM74C904 (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = 0V	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = 0V	3.8			mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C901/MM74C901, MM54C903/MM74C903					
Input Capacitance (C_{IN})	Any Input (Note 2)		14		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		38 22	70 30	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		21 13	35 20	ns ns
MM54C902/MM74C902, MM54C904/MM74C904					
Input Capacitance (C_{IN})	Any Input (Note 2)		5.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		50		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		57 27	90 40	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		54 25	90 40	ns ns

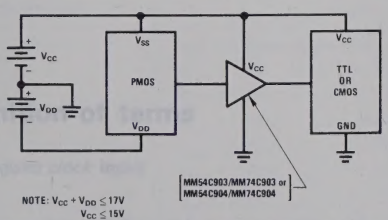
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

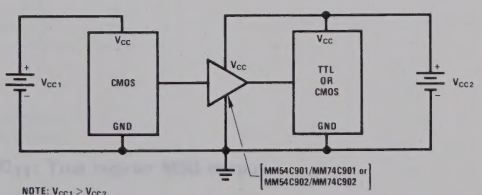
typical applications

PMOS to CMOS or TTL Interface



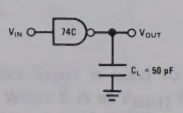
NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



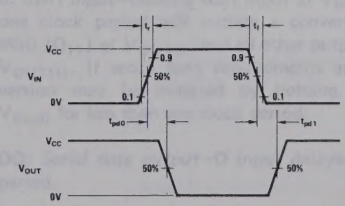
NOTE: $V_{CC1} \geq V_{CC2}$

ac test circuit and switching time waveforms



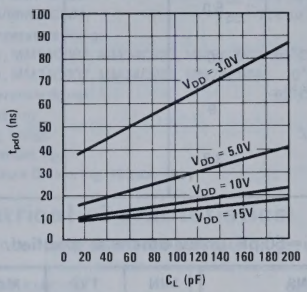
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

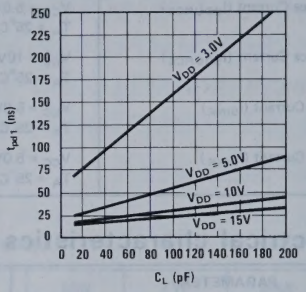


typical performance characteristics

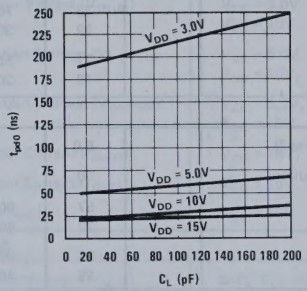
Typical Propagation Delay to a Logical "0" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



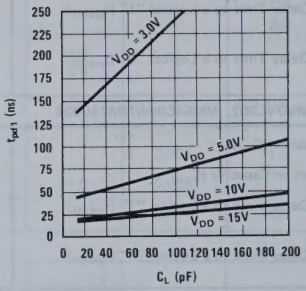
Typical Propagation Delay to a Logical "1" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



Typical Propagation Delay to a Logical "0" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



Typical Propagation Delay to a Logical "1" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



MM54C905/MM74C905 12-bit successive approximation register

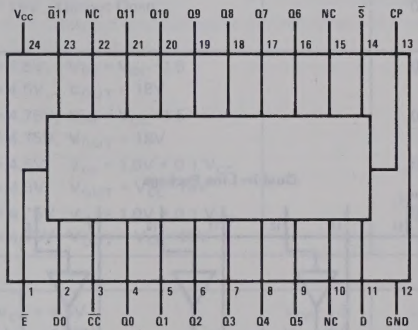
general description

The MM54C905/MM74C905, CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power fan out of 2
  TTL compatibility driving 74L
- Provisions for register extension or truncation
- Operates in start/stop or continuous conversion mode
- Drives ladder switches directly

connection diagram


V_{CC} $\overline{Q11}$ NC Q11 Q10 Q9 Q8 Q7 Q6 NC $\overline{S}$ CP
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
$\overline{E}$ D0 $\overline{CC}$ Q0 Q1 Q2 Q3 Q4 Q5 NC D GND

MM54C905/MM74C905
12-Bit Successive Approximation Register

definition of terms

CP: Register *clock* input

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q_{11} is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q_{11}: True register MSB output.

$\overline{Q}_{11}$: Complement of register MSB output.

Qi (i=0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q_{11}) at $V_{OUT(0)}$ and all other output (Q_{10}-Q_0) at $V_{OUT(1)}$. If setup time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Advance Information

MM54C906/MM74C906 hex open drain N-channel buffers
MM54C907/MM74C907 hex open drain P-channel buffers

general description

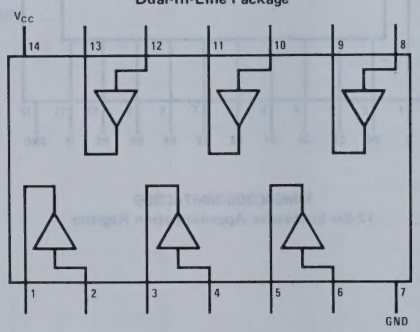
These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up 0V pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- High current sourcing and sinking open drain outputs

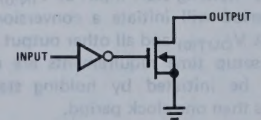
connection diagram

Dual-In-Line Package

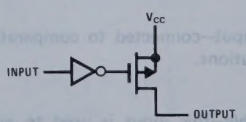


MM54C906/MM74C906
MM54C907/MM74C907

logic diagrams



MM54C906/MM74C906



MM54C907/MM74C907

absolute maximum ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Output Pin	
MM54C906/MM74C906	−0.3V to +18V
MM54C907/MM74C907	V_{CC} − 18V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C906/MM54C907	−55°C to +125°C
MM74C906/MM74C907	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Output Open		0.05	15	μA
Output Leakage					
MM54C906	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = 18V				
MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = 18V				
MM54C907	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−18V				
MM74C907	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−18V				
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE CURRENT					
MM54C906	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.5V, V_{OUT} = 0.5V		8		mA
	V_{CC} = 4.5V, V_{OUT} = 1.0V		12		mA
MM74C906	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.75V, V_{OUT} = 0.5V		8		mA
	V_{CC} = 4.75V, V_{OUT} = 1.0V		12		mA
MM54C907	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−0.5V		1.5		mA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−1.0V		3.0		mA
MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−0.5V		1.5		mA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−1.0V		3.0		mA
MM54C906/MM74C906	V_{CC} = 10V, V_{IN} = 2.0V				
	V_{CC} = 10V, V_{OUT} = 0.5V		20		mA
	V_{CC} = 10V, V_{OUT} = 1.0V		30		mA
MM54C907/MM74C907	V_{CC} = 10V, V_{IN} = 8.0V				
	V_{CC} = 10V, V_{OUT} = 9.5V		4.0		mA
	V_{CC} = 10V, V_{OUT} = 9.0V		8.0		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "0" (t_{pd0})					
MM54C906/MM74C906	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
MM54C907/MM74C907	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V, (Note 4)			75 + 0.7 RC	ns
Propagation Delay to a Logical "1" (t_{pd1})					
MM54C906/MM74C906	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V (Note 4)			75 + 0.7 RC	ns
MM54C907/MM74C907	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
Input Capacity (C_{IN})	(Note 2)		5		pF
Output Capacity (C_{OUT})	(Note 2)		20		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

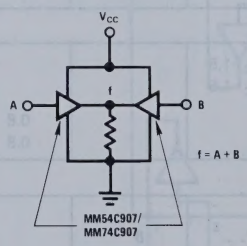
Note 2: Capacitance is guranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes output avenue open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

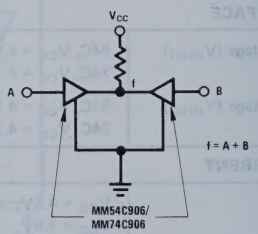
typical applications

Wire OR Gate



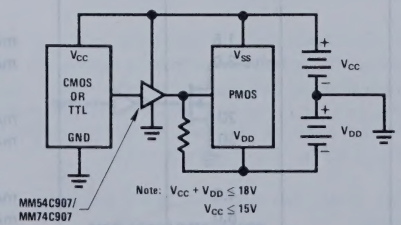
Note: Can be extended to more than 2 inputs.

Wire AND Gate

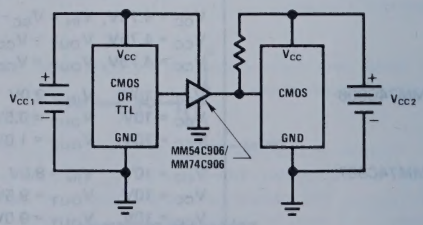


Note: Can be extended to more than 2 inputs.

CMOS or TTL to PMOS Interface



CMOS or TTL to CMOS at a Higher V_{CC}



MM54C908/MM74C908 dual high voltage CMOS driver

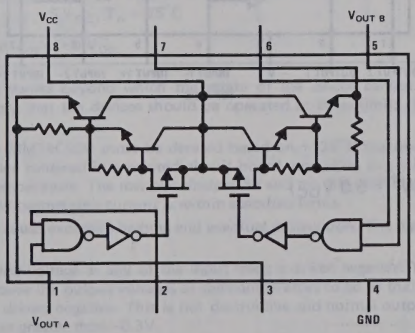
general description

The MM54C908/MM74C908 consists of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, etc.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Output source current	250 mA typ at $V_{OUT} = V_{CC} - 3V$
■ High voltage output	50V typ

connection diagram



MM54C908/MM74C908
Dual High Voltage Driver

MM54C909/MM74C909 quad comparator

general description

The MM54C909/MM74C909 contains four independent voltage comparators designed to operate from standard 54C/74C power supplies. The output allows current sinking only thus the wire OR function is possible using a common resistor pull up.

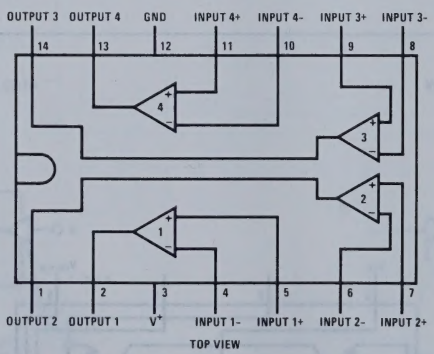
Not only does the MM54C909/MM74C909 function as a comparator for analog inputs but also has many applications as a voltage translator and buffer when interfacing the 54C/74C family to other logic systems.

features

■ Wide supply voltage range	3.0V to 15V
■ TTL compatibility	fan out of 1 driving 74
■ Low power consumption	I_{CC} = 800μA typ at V_{CC} = 5.0 V_{DC}
■ Low input bias current	250 nA max
■ Low input offset current	±50 nA max
■ Low input offset voltage	±5.0 mV max
■ Large common mode input voltage range	0V to V_{CC}−1.5V
■ Large differential input voltage range	V_{CC}

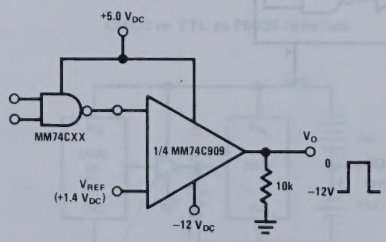
connection diagram

Dual-In-Line and Flat Package

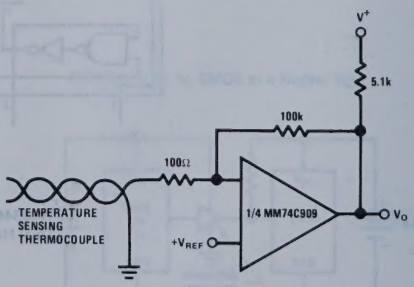


TOP VIEW

typical applications (V^+ = 5.0 V_{DC})



CMOS/TTL to MOS Logic Converter



Ground Referenced Thermocouple in Single Supply System

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C909	−55°C to +125°C
MM74C909	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (Notes 2 and 3)	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Input Current ($V_{IN} < -0.3V$) (Note 4)	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted. (V_{CC} = +5.0 V_{DC})

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 9)				±9	mV
	T_A = 25°C		±2	±5	mV
Input Bias Current ($I_{IN(+)}$ or $I_{IN(-)}$) (Note 5)	T_A = 25°C, With Output in Linear Range		25	250 400	nA nA
Input Offset Current ($I_{IN(+)} - I_{IN(-)}$)	T_A = 25°C		±5	±150 ±50	nA nA
Input Common Mode Voltage (Note 6)		0		V_{CC}−2	V
	T_A = 25°C	0		V_{CC}−1.5	V
Supply Current (I_{CC})	T_A = 25°C, R_L = ∞ On All Outputs		800	2000	μA
Voltage Gain	T_A = 25°C, $R_L \geq$ 15 kΩ		200		V/mV
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Sink Current (I_{SINK})					
MM54C909	V_{CC} = 4.50V	1.6	3.2		mA
MM74C909	V_{CC} = 4.75V, V_{OUT} = 0.4V				
	$V_{IN(-)} \geq$ 1.0 V_{DC} $V_{IN(+)}$ = 0 V_{DC}				
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V_{OUT} = 15 V_{DC}			1	μA
	$V_{IN(+)} \geq$ 1.0 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V_{OUT} = 5 V_{DC}, T_A = 25°C		0.1		nA
Differential Input Voltage (Note 8)	All V_{IN}'s $\geq$ 0 V_{DC}			15	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operating at high temperatures, the MM74C909 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies to the device soldered in a printed circuit board, operating in a still air ambient. The MM54C909 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output sink current is within specified limits.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. There is a lateral NPN parasitic transistor action on the IC chip. The transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 5: The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +15V without damage.

Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can equal V_{CC} supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V.

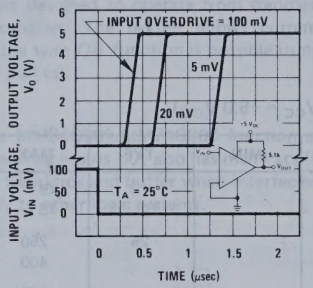
Note 9: At output switch point, V_O = 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC} and over the full input common mode range (0V_{DC}) to V^+ ±1.5 V_{DC}).

ac electrical characteristics $R_L = 5.1\ k\Omega$, $V_{RL} = 5.0\ V_{DC}$, unless otherwise specified.

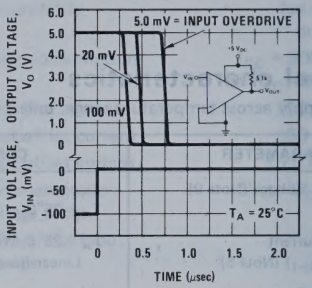
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Response Time	V_{IN} = TTL Swing $V_{REF} = 1.4\ V_{DC}$		300		ns
Response Time	$T_A = 25°C$		1.3		μs

typical performance characteristics

Response Time for Various Input Overdrives — Positive Transition



Response Time for Various Input Overdrives — Negative Transition



application hints

The MM54C909/MM74C909 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $<10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

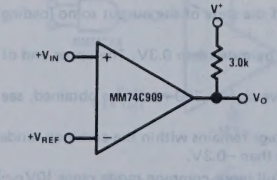
The bias network of the MM54C909/MM74C909 establishes an I_{CC} current which is independent of the magnitude of the power supply voltage over the range of from 3.0V to 15V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

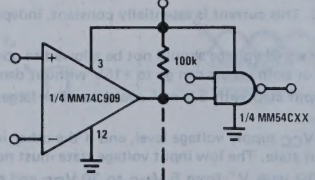
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

Many outputs can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the MM54C909/MM74C909 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the gain of the output device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly.

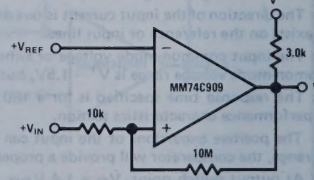
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



Basic Comparator

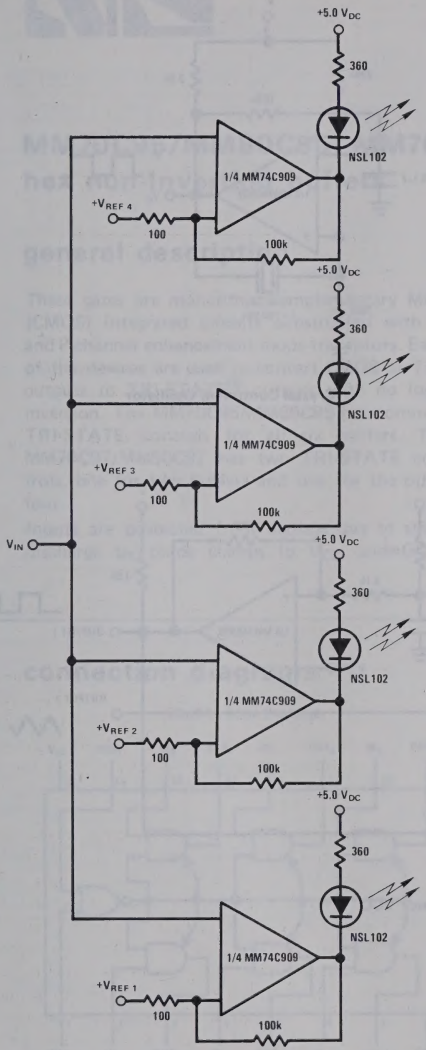


Driving CMOS

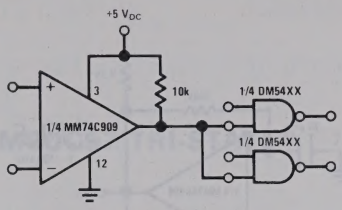


Non-Inverting Comparator with Hysteresis

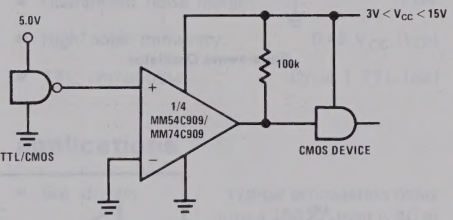
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



Visible Voltage Indicator

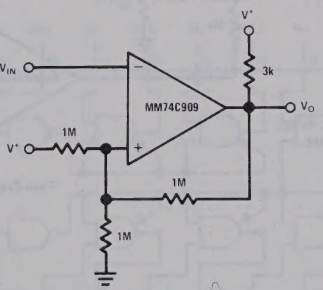


Driving TTL

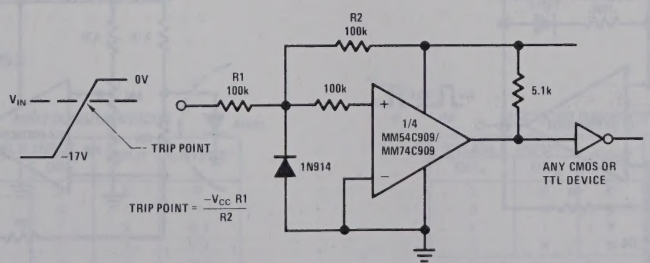


Note: For inverting buffer reverse input connection.

5V Logic to CMOS Operating at $V_{CC} \neq 5V$



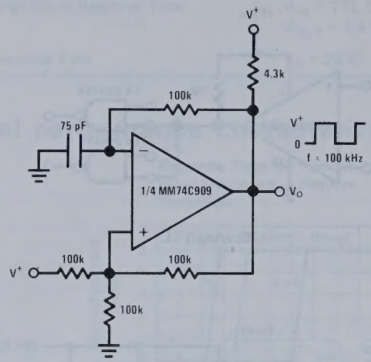
Inverting Comparator with Hysteresis



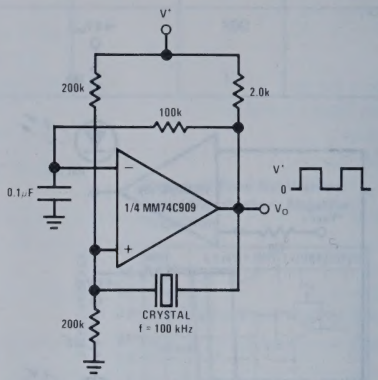
Note: For non-inverting buffer reverse input connection.

Hi Voltage Inverting PMOS to CMOS or TTL

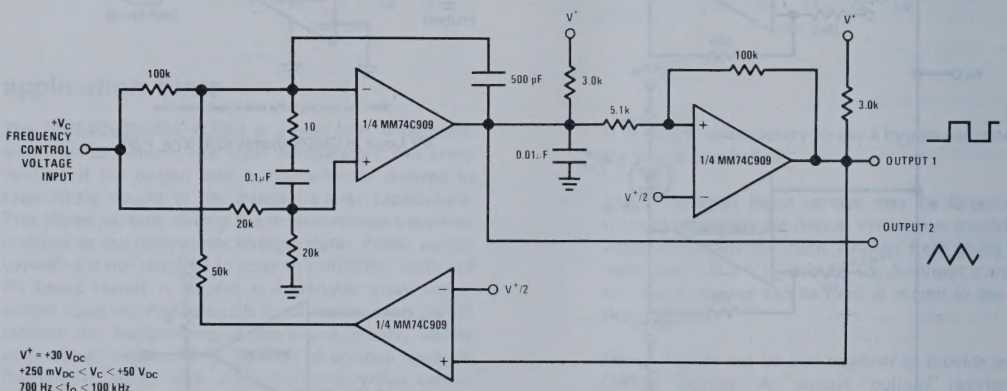
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



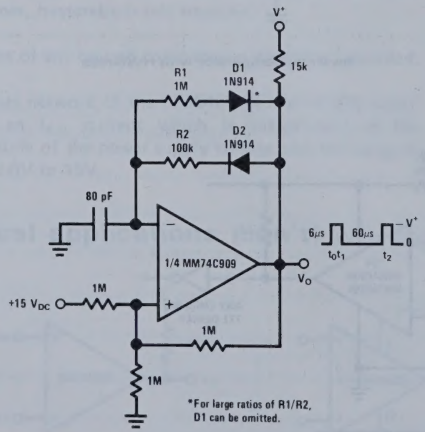
Squarewave Oscillator



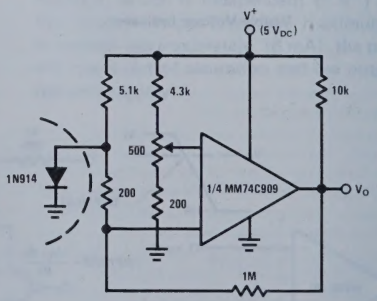
Crystal Controlled Oscillator



Two-Decade High-Frequency VCO



Pulse Generator



Remote Temperature Sensing

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® hex non-inverting buffers

general description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each of the devices are used to convert CMOS or TTL outputs to TRI-STATE® outputs with no logic inversion. The MM70C95/MM80C95 has common TRI-STATE controls for all six buffers. The MM70C97/MM80C97 has two TRI-STATE controls, one for two buffers and one for the other four.

Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

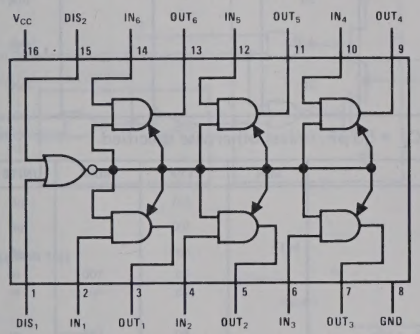
- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ)
- TTL compatible — Drive 1 TTL load

applications

- Bus drivers — typical propagation delay into a 150 pF load is 40 ns

connection diagrams

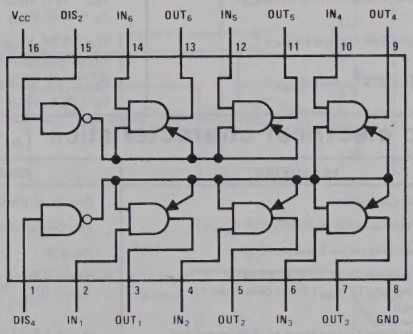
Dual-In-Line Package



TOP VIEW

MM70C95/MM80C95

Dual-In-Line Package



TOP VIEW

MM70C97/MM80C97

truth tables

MM70C95/MM80C95

DISABLE INPUT		INPUT	OUTPUT
DIS_1	DIS_2		
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE INPUT		INPUT	OUTPUT
DIS_4	DIS_2		
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only
**Output 1-4 only
X = Irrelevant

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
MM70C95, MM70C97	−55°C to +125°C	Power Supply Voltage, V_{CC}	16V
MM80C95, MM80C97	0°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10V	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10V			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)		−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	70C V_{CC} = 4.5V	V_{CC} − 1.5			V
	80C V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	70C V_{CC} = 4.5V			0.8	V
	80C V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	70C V_{CC} = 4.5V, I_0 = −1.6 mA	2.4			V
	80C V_{CC} = 4.75V, I_0 = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	70C V_{CC} = 4.5V, I_0 = 1.6 mA			0.4	V
	80C V_{CC} = 4.75V, I_0 = 1.6 mA			0.4	V
OUTPUT DRIVE CURRENT					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = 0V	−4.35			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = 0V	−20			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = V_{CC}	4.35			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, V_{IN} = 0V T_A = 25°C, V_{OUT} = V_{CC}	20			mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

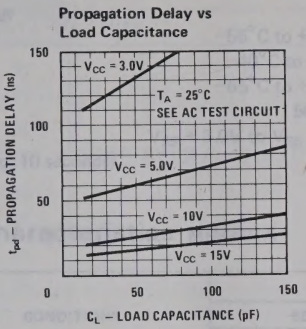
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	Any Input (Note 2)		5.0		pF
Output Capacitance TRI-STATE (C_{OUT})	Any Output (Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		60		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Data Input to Output	V_{CC} = 5.0V		60	100	ns
	V_{CC} = 10V		25	40	ns
Delay From Disable Input to High Impedance State (From Logical "1" or Logical "0" Level) (t_{1H}, t_{0H}) MM70C95/MM80C95	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		80	135	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		50	90	ns
Delay From Disable Input to Logical "1" Level (t_{H1}) or to Logical "0" Level (t_{H0}) (From High Impedance State) MM70C95/MM80C95	V_{CC} = 5.0V, C_L = 50 pF, R_L = 10k		120	200	ns
	V_{CC} = 10V, C_L = 50 pF, R_L = 10k		50	90	ns
Delay From Disable Input to High Impedance State (From Logical "1" or Logical "0" Level) (t_{1H}, t_{0H}) MM70C97/MM80C97	V_{CC} = 5.0V, R_L = 10k		70	125	ns
	V_{CC} = 10V, R_L = 10k		50	90	ns
Delay From Disable Input to Logical "1" Level (t_{H1}) or to Logical "0" Level (t_{H0}) (From High Impedance State) MM70C97/MM80C97	V_{CC} = 5.0V, R_L = 10k		95	175	ns
	V_{CC} = 10V, R_L = 10k		40	80	ns
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Data Input to Output	V_{CC} = 5.0V, C_L = 150 pF, T_A = 25°C		85	160	ns
	V_{CC} = 10V, C_L = 150 pF, T_A = 25°C		40	80	ns

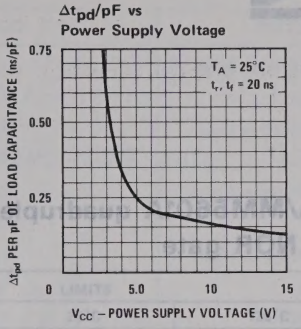
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

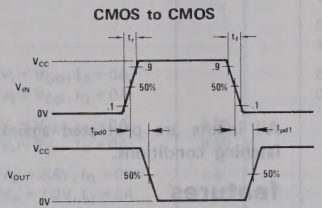
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

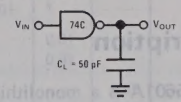
typical performance characteristics





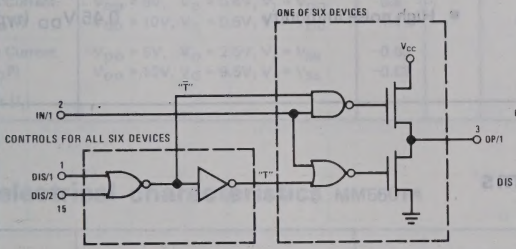
ac test circuits and switching time waveforms



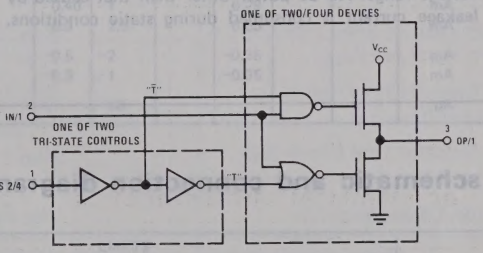


(For TRI-STATE® Parameters)

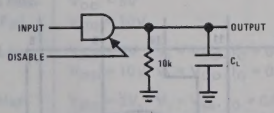
MM70C95/MM80C95 TRI-STATE

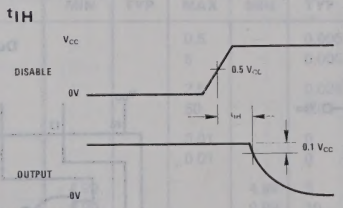


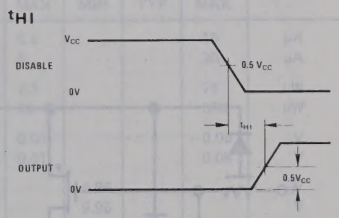
MM70C97/MM80C97



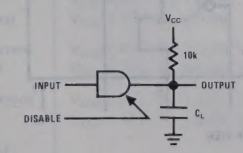
t_{IH} and t_{HI}

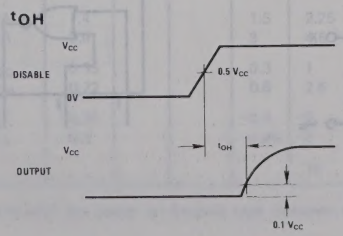


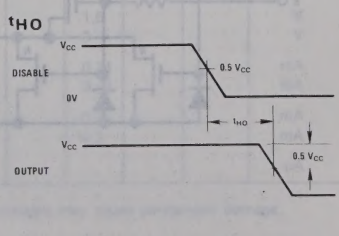




t_{OH} and t_{HO}







Note: Delays measured with input t_r, $t_f \leq 20$ ns.

MM4601A/MM5601A quadruple two-input NOR gate

general description

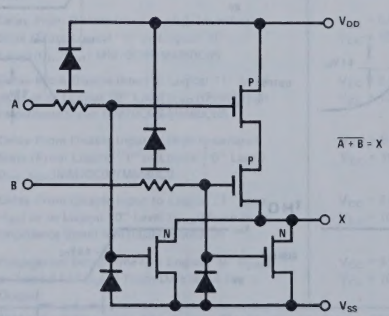
The MM4601A/MM5601A is a monolithic complementary MOS (CMOS) quadruple two-input NOR gate integrated circuit. N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions.

All inputs are protected against static discharge and latching conditions.

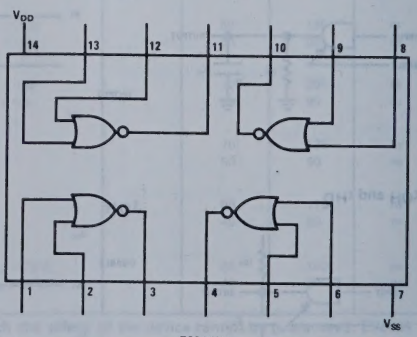
features

- Wide supply voltage range — 3V to 15V
- Low power — 10 nW (typ)
- High noise immunity — 0.45 V_{DD} (typ)

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	
MM4601A	−55°C to +125°C
MM5601A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4601A

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			0.05		0.001	0.05			3	μA
	$V_{DD} = 10V$			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			0.25		0.005	0.25			15	μW
	$V_{DD} = 10V$			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$, $V_I = V_{DD}$, $I_O = 0A$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$, $V_I = V_{SS}$, $I_O = 0A$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$, $V_O = 3.6V$, $I_O = 0A$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$, $V_O = 0.95V$, $I_O = 0A$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.5			0.40	1		0.28			mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.1			0.9	2.5		0.65			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.62			−0.5	−2		−0.35			mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62			−0.5	−1		−0.35			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5601A

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			0.5		0.005	0.5			15	μA
	$V_{DD} = 10V$			5		0.005	5			30	μA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			2.5		0.025	2.5			75	μW
	$V_{DD} = 10V$			50		0.05	50			300	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$, $V_I = V_{DD}$, $I_O = 0A$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$, $V_I = V_{SS}$, $I_O = 0A$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$, $V_O = 3.6V$, $I_O = 0A$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$, $V_O = 0.95V$, $I_O = 0A$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.35			0.3	1		0.24			mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.35			−0.3	−2		−0.24			mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.3			−0.25	−1		−0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics MM4601A

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5V$		35	65	ns
	$V_{DD} = 10V$		25	40	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5V$		35	65	ns
	$V_{DD} = 10V$		25	40	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
Input Capacitance (C_I)	Any Input		5		pF

dynamic electrical characteristics MM5601A

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
Input Capacitance (C_I)	Any Input		5		pF

MM4602A/MM5602A dual four-input NOR gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

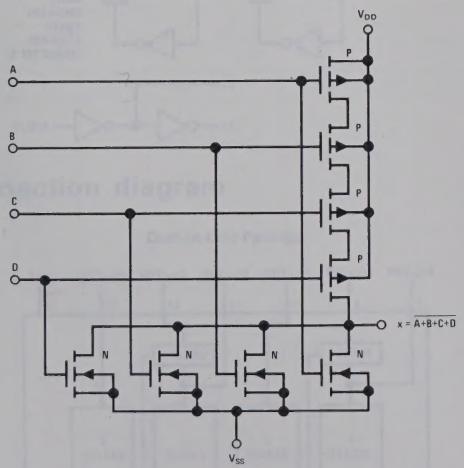
features

- Wide supply voltage range 3V to 15V
- Low power 10 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)

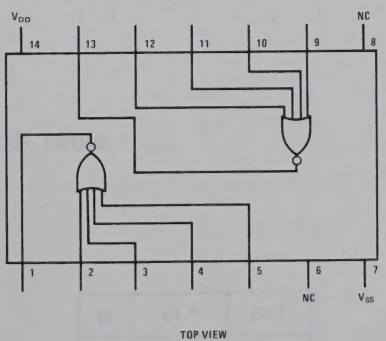
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} −0.3V to V_{SS} +15.5V	Package Dissipation	500 mW
Operating Temperature Range MM4602A	−55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
MM5602A	−40°C to +85°C	Operating V_{DD} Range	V_{SS} +3V to V_{SS} +15V
Storage Temperature Range	−65°C to +150°C		

electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																UNITS
			MM4602AD, MM4602AF									MM5602AN							
			−55°C			25°C			125°C			−40°C			25°C			85°C		
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	0.5	–	0.001	0.05	–	–	3	–	–	0.5	–	0.005	0.5	–	–	15	μA
		10	–	–	0.1	–	0.001	0.1	–	–	6	–	–	5	–	0.005	5	–	–	30	
Quiescent Device Dissipation/Package (P_D)		5	–	–	0.25	–	0.005	0.25	–	–	15	–	–	2.5	–	0.025	2.5	–	–	75	μW
		10	–	–	1	–	0.01	1	–	–	60	–	–	50	–	0.05	50	–	–	300	
Output Voltage Low Level (V_{OL})		5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	
High Level (V_{OH})		5	4.99	–	–	4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
		10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NI})	$V_O > 3.5$	5	1.5	–	–	1.5	2.25	–	1.4	–	–	1.5	–	–	1.5	2.25	–	1.4	–	–	V
	$V_O > 7.0$	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O < 1.5$	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O < 3.0$	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current N-Channel (I_DN)	0.4	5	0.5	–	–	0.40	–	–	0.28	–	–	0.35	–	–	0.3	1	–	0.24	–	–	mA
	$V_I = V_{DD}$ 0.5	10	1.1	–	–	0.9	–	–	0.65	–	–	0.72	–	–	0.6	2.5	–	0.48	–	–	
P-Channel (I_DP)	2.5	5	−0.62	–	–	−0.5	–	–	−0.35	–	–	−0.35	–	–	−0.3	−2	–	−0.24	–	–	mA
	$V_I = V_{SS}$ 9.5	10	−0.62	–	–	−0.5	–	–	−0.35	–	–	−0.3	–	–	−0.25	−1	–	−0.2	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		MM4602AD MM4602AF			MM5602AN			
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time:	5	–	35	50	–	35	80	ns
Low-to-High Level (t_{PLH})	10	–	25	40	–	25	55	
High-to-Low Level (t_{PHL})	5	–	35	95	–	35	120	ns
	10	–	25	45	–	25	65	
Transition Time:	5	–	65	125	–	65	200	ns
Low-to-High Level (t_{TLH})	10	–	35	70	–	35	115	
High-to-Low Level (t_{THL})	5	–	65	175	–	65	300	ns
	10	–	35	75	–	35	125	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

MM4606A/MM5606A 18-stage static shift register

general description

The MM4606A/MM5606A 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register section of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

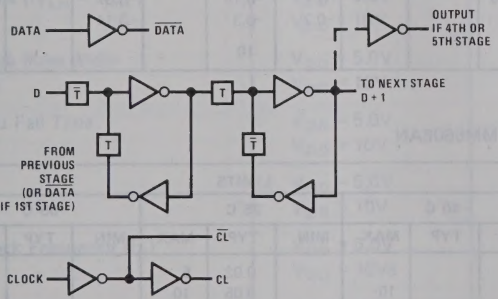
features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low clock input capacitance	6 pF typ
■ Medium speed operation	10 MHz typ with V_{DD} = 10V
■ Low power	
■ Fully static operation	

applications

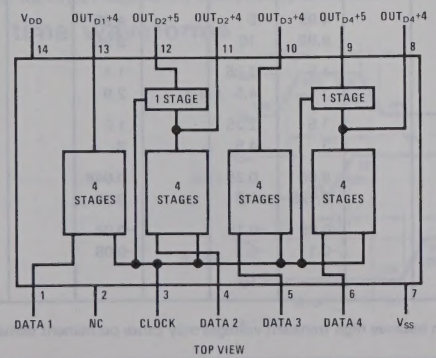
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industry control
- Remote metering
- Computers

logic diagrams



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

D	CL$^{\Delta}$	D+1
0	⌐	0
1	⌐	1
X	⌐	NC

X = Don't care
Δ = Level change
NC = No change

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
MM4606A	−55°C to +125°C
MM5606A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4606AD, MM4606AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.01	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			2.5		0.05	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99				4.99	5	4.95			V
	V_{DD} = 10V	9.99				9.99	10	9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.155			0.125	0.25		0.085			mA
	V_{DD} = 10V, V_O = 0.5V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.125			−0.1	−0.15		−0.07			mA
	V_{DD} = 10V, V_O = 9.5V	−0.25			−0.2	−0.3		−0.14			mA
Input Current (I_I)	Any Input					10					pA

static electrical characteristics MM5606AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5		0.03	5			70	μA
	V_{DD} = 10V			10		0.05	10			140	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		0.15	25			350	μW
	V_{DD} = 10V			100		0.5	100			1400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.072			0.06	0.25		0.048			mA
	V_{DD} = 10V, V_O = 0.5V	0.15			0.125	0.5		0.10			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.06			−0.05	−0.15		−0.04			mA
	V_{DD} = 10V, V_O = 9.5V	−0.12			−0.1	−0.3		−0.08			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics

MM4606AD, MM4606AF at $T_A = 25^\circ C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^\circ C$.

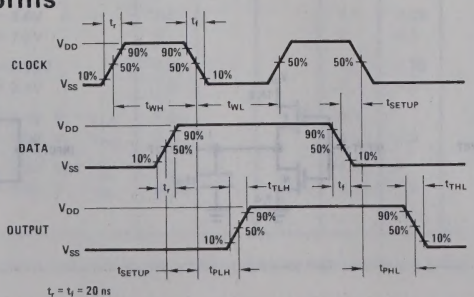
PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5.0V$		180	400	ns
	$V_{DD} = 10V$		80	200	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5.0V$		150	400	ns
	$V_{DD} = 10V$		60	200	ns
Minimum Clock Pulse Width ($T_{WL} = T_{WH}$)	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	200	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			5	μs
Set-Up Time	$V_{DD} = 5.0V$		50	80	ns
	$V_{DD} = 10V$		25	40	ns
Maximum Clock Frequency (f_{cl})	$V_{DD} = 5.0V$	1	5		MHz
	$V_{DD} = 10V$	2.5	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

dynamic electrical characteristics MM5606AN

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5.0V$		180	500	ns
	$V_{DD} = 10V$		80	250	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5.0V$		150	400	ns
	$V_{DD} = 10V$		60	250	ns
Minimum Clock Pulse Width ($T_{WH} = T_{WL}$)	$V_{DD} = 5.0V$		100	830	ns
	$V_{DD} = 10V$		50	250	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			5	μs
Set-Up Time	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
Maximum Clock Frequency (f_{cl})	$V_{DD} = 5.0V$	0.6	5		MHz
	$V_{DD} = 10V$	2	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

*If more than one unit is cascaded t_{rCl} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output stage for the estimated capacitive load.

switching time waveforms



MM4607A/MM5607A dual complementary pair plus inverter

general description

The MM4607A/MM5607A consists of three complementary pairs of N-channel and P-channel enhancement mode MOS transistors. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

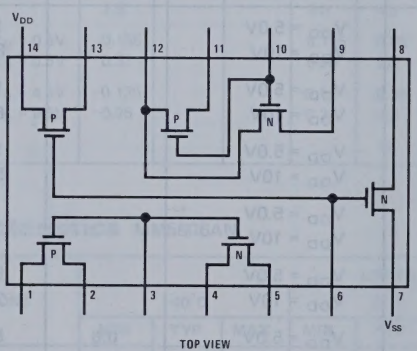
For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ at all times.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ

connection diagram

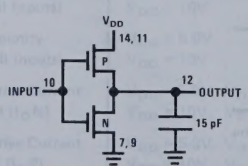
Dual-In-Line and Flat Package

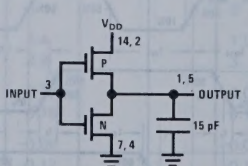


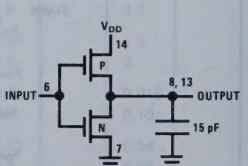
TOP VIEW

Note: All P-channel substrates are connected to V_{DD}, and all N-channel substrates are connected to V_{SS}.

ac test circuits







absolute maximum ratings (Note 1)

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	
MM4607A	−55°C to +125°C
MM5607A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4607A

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			0.05		0.001	0.05			3	μA
	$V_{DD} = 10V$			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			0.25		0.005	0.25			15	μW
	$V_{DD} = 10V$			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$, $V_O = 3.6V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 7.2V$	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$, $V_O = 0.95V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 2.9V$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.75			0.6	1		0.4			mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.6			1.3	2.5		0.95			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 2.5V$, $V_I = V_{SS}$	−1.75			−1.4	−4		−1			mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−1.35			−1.1	−2.5		−0.75			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5607A

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			0.5		0.005	0.5			15	μA
	$V_{DD} = 10V$			1		0.005	1			30	μA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			2.5		0.025	2.5			75	μW
	$V_{DD} = 10V$			10		0.05	10			300	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$, $V_O = 3.6V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 7.2V$	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$, $V_O = 0.95V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 2.9V$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.35			0.3	1		0.24			mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.2			1	2.5		0.8			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 2.5V$, $V_I = V_{SS}$	−1.3			−1.1	−4		−0.9			mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.65			−0.55	−2.5		−0.45			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics MM4607A

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

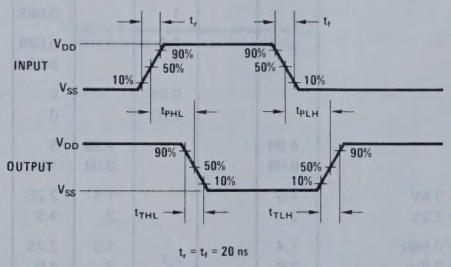
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5V$		35	60	ns
	$V_{DD} = 10V$		20	40	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5V$		50	75	ns
	$V_{DD} = 10V$		30	40	ns
Input Capacitance (C_I)	Any Input		5		pF

dynamic electrical characteristics MM5607A

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5V$		35	75	ns
	$V_{DD} = 10V$		20	50	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5V$		50	100	ns
	$V_{DD} = 10V$		30	50	ns
Input Capacitance (C_I)	Any Input		5		pF

switching time waveforms



$t_r = t_f = 20$ ns

MM4609A/MM5609A hex buffers (inverting)
MM4610A/MM5610A hex buffers (non-inverting)

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

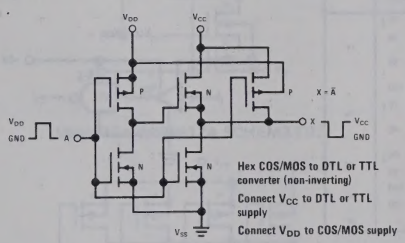
features

- Wide supply voltage range 3V to 15V
- Low power 100 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)
- High current sinking capability 8 mA (min) at VO = 0.5V and V_{DD} = 10V

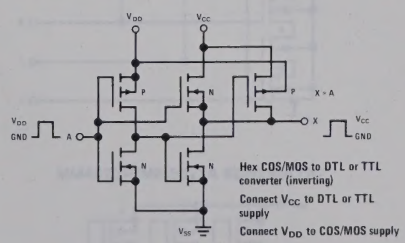
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

schematic and connection diagrams

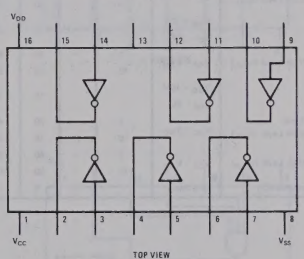


MM4609A/MM5609A

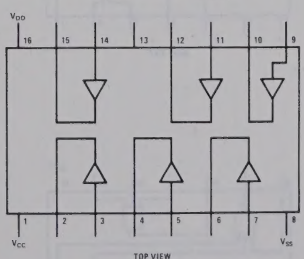


MM4610A/MM5610A

Dual-In-Line Package



Dual-In-Line Package



absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V	Package Dissipation	500 mW
Operating Temperature Range MM46XXA	–55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
MM56XXA	–40°C to +85°C	Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Storage Temperature Range	–65°C to +150°C		

static electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																UNITS
			MM4609AD, MM4609AF, MM4610AD, MM4610AF									MM5609AN, MM5610AN							
			–55°C			25°C			125°C			–40°C			25°C			85°C		
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current: (I_L)		5	–	–	0.3	–	0.01	0.3	–	–	20	–	–	3	–	0.03	3	–	–	42	μA
		10	–	–	0.5	–	0.01	0.5	–	–	30	–	–	5	–	0.05	5	–	–	70	
Quiescent Device Dissipation/Package (P_D)		5	–	–	1.5	–	0.05	1.5	–	–	100	–	–	15	–	0.15	15	–	–	210	μW
		10	–	–	5	–	0.1	5	–	–	300	–	–	50	–	0.5	50	–	–	700	
Output Voltage: Low-Level (V_{OL})		5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	
High-Level (V_{OH})		5	4.99	–	–	4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
		10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs)																					
(V_{NL}) MM4609 Series	$V_O \geq 4.0$	5	1	–	–	1	2.25	–	0.9	–	–	1	–	–	1	2.25	–	0.9	–	–	
	$V_O \geq 8.0$	10	2	–	–	2	4.5	–	1.2	–	–	2	–	–	2	4.5	–	1.9	–	–	
(V_{NL}) MM4610A Series	$V_O \leq 1.5$	5	1.6	–	–	1.5	2.25	–	1.4	–	–	1.6	–	–	1.5	2.25	–	1.4	–	–	V
	$V_O \leq 3.0$	10	3.2	–	–	3	4.5	–	2.9	–	–	3.2	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O \geq 3.5$	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O \geq 7.0$	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current: N-Channel ($I_D N$)	0.4	5	3.75	–	–	3	4	–	2.1	–	–	3.6	–	–	3	–	–	2.4	–	–	mA
	0.5	10	10	–	–	8	10	–	5.6	–	–	9.6	–	–	8	–	–	6.4	–	–	
P-Channel ($I_D P$)	2.5	5	–1.85	–	–	–1.25	–1.75	–	–0.9	–	–	–1.5	–	–	–1.25	–	–	–1	–	–	mA
	9.5	10	–0.9	–	–	–0.6	–0.8	–	–0.4	–	–	–0.72	–	–	–0.6	–	–	–0.48	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

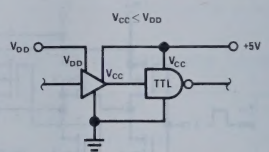
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

dynamic electrical characteristics at $T_A = 25°C$ and $C_L = 15$ pF

Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			MM4609AD, MM4609AF MM4610AD, MM4610AF			MM5609AN, MM5610AN			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: High-to-Low Level (t_{PHL})	$V_{CC} = V_{DD}$	5	–	15	55	–	15	70	ns
		10	–	10	30	–	10	40	
	$V_{DD} = 10V$ $V_{CC} = 5V$		–	10	25	–	10	35	
Low-to-High Level (t_{PLH})	$V_{CC} = V_{DD}$	5	–	50	80	–	50	100	ns
		10	–	25	55	–	25	70	
	$V_{DD} = 10V$ $V_{CC} = 5V$		–	15	30	–	15	40	
Transition Time: High-to-Low Level (t_{THL})	$V_{CC} = V_{DD}$	5	–	20	45	–	20	60	ns
		10	–	16	40	–	16	50	
Low-to-High Level (t_{TLH})	$V_{CC} = V_{DD}$	5	–	80	125	–	80	160	ns
		10	–	50	100	–	50	120	
Input Capacitance (C_I)	Any Input		–	5	–	–	5	–	pF

typical applications



MM4611A/MM5611A quad two-input NAND gate
MM4612A/MM5612A dual four-input NAND gate
MM4623A/MM5623A triple three-input NAND gate

general description

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

features

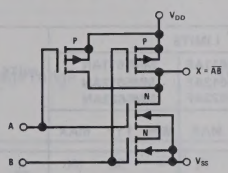
- Wide supply voltage range 3V to 15V
- Low power 10 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)

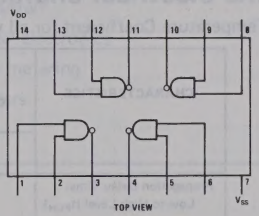
applications

- Automotive
- Data Terminals
- Instrumentation
- Medical Electronics
- Alarm System
- Industrial Controls
- Remote Metering
- Computers

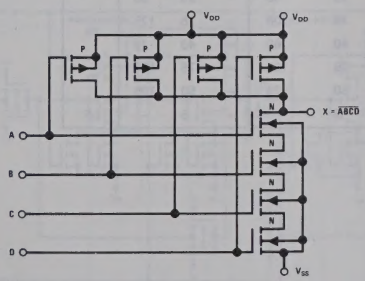
schematic and connection diagrams

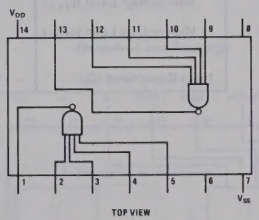
MM4611A/MM5611A SCHEMATIC



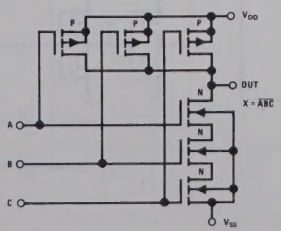


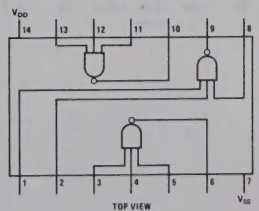
MM4612A/MM5612A SCHEMATIC





MM4623A/MM5623A SCHEMATIC





absolute maximum ratings

Voltage at Any Pin (Note 1)		V_{SS} – 0.3V to V_{SS} + 15.5V	
Operating Temperature Range	MM46XXA	–55°C to +125°C	
	MM56XXA	–40°C to +85°C	
Storage Temperature Range		–65°C to +150°C	
Package Dissipation			500 mW
Lead Temperature (Soldering, 10 sec)			300°C
Operating V_{DD} Range			V_{SS} + 3V to V_{SS} + 15V

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

static electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS: MM4611AD, MM4611AF, MM4612AD, MM4612AF, MM4623AD, MM4623AF									LIMITS: MM5611AN, MM5612AN, MM5613.									UNITS
			–55°C			25°C			125°C			–40°C			25°C			85°C			
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	0.05	–	0.001	0.05	–	–	3	–	–	0.5	–	0.005	0.5	–	–	15	µA
		10	–	–	0.1	–	0.001	0.1	–	–	6	–	–	5	–	0.005	5	–	–	30	
Quiescent Device Dissipation/Package (P_D)		5	–	–	0.25	–	0.005	0.25	–	–	15	–	–	2.5	–	0.025	2.5	–	–	75	µW
		10	–	–	1	–	0.01	1	–	–	60	–	–	50	–	0.05	50	–	–	300	
Output Voltage Low-Level (V_{OL})		5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	
High-Level (V_{OH})		5	4.99	–	–	4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
		10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NL})	$V_O \geq 3.5$	5	1.5	–	–	1.5	2.25	–	1.4	–	–	1.5	–	–	1.5	2.25	–	1.4	–	–	V
	$V_O \geq 7.0$	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O \leq 1.5$	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O \leq 3.0$	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current N-Channel (I_DN)	0.5	5	0.31	–	–	0.25	0.5	–	0.175	–	–	0.145	–	–	0.12	0.5	–	0.95	–	–	mA
	0.5	10	0.62	–	–	0.5	0.6	–	0.35	–	–	0.3	–	–	0.25	0.6	–	0.2	–	–	
P-Channel (I_DP)	4.5	5	–0.31	–	–	–0.25	–0.5	–	–0.175	–	–	–0.145	–	–	–0.12	–0.5	–	–0.95	–	–	mA
	9.5	10	–0.75	–	–	–0.6	–1.2	–	–0.4	–	–	–0.35	–	–	–0.3	–1.2	–	–0.24	–	–	
Input Current (I_I)				–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

dynamic electrical characteristics @ $T_A = 25°C$ and $C_L = 15pF$

Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS: MM4611AD MM4612AD MM4623AD MM4611AF MM4612AF MM4623AF			LIMITS: MM5611AN MM5612AN MM5623AN			UNITS
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: Low-to-High Level (t_{PLH})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
High-to Low Level (t_{PHL})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
Transition Time: Low-to-High Level (t_{TLH})	5	–	75	100	–	75	125	ns
	10	–	40	60	–	40	75	
High-to-Low Level (t_{THL})	5	–	75	125	–	75	150	ns
	10	–	50	75	–	50	100	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

MM4613A/MM5613A dual D flip-flop

general description

The MM4613A/MM5613A dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P channel enhancement transistors. Each flip flop has independent data, set, reset, and clock inputs and, "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and, by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transfered to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

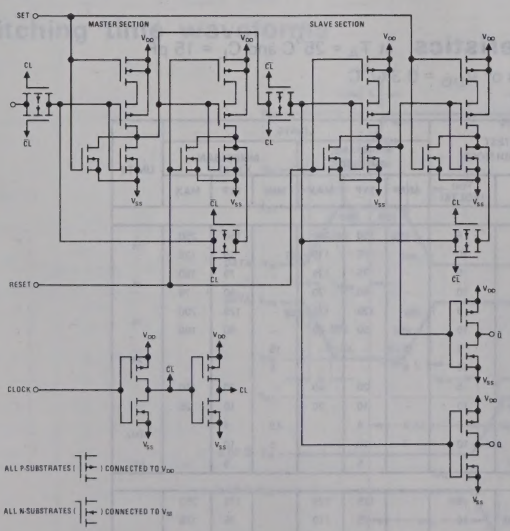
features

- Supply voltage range — 3V to 15V
- Noise Immunity — 0.45 V_{DD} (typ)
- Low power — 50 nW (typ)
- Medium speed operation — 10 MHz (typ) with 10 volt supply

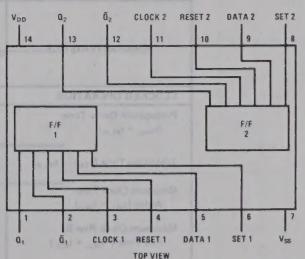
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

schematic and connection diagrams



Dual-In-Line Package


V_{DD} Q_2 $\overline{Q}_2$ CLOCK 2 RESET 2 DATA 2 SET 2
14 13 12 11 10 9 8
F/F 1
F/F 2
1 2 3 4 5 6 7
Q_1 $\overline{Q}_1$ CLOCK 1 RESET 1 DATA 1 SET 1 V_{SS}
TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM46XXA	−55°C to +125°C
MM56XXA	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

static electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																UNITS
			MM4613AD, MM4613AF									MM5613AN							
			−55°C			25°C			125°C			−40°C			25°C			85°C		
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	1	–	0.005	1	–	–	60	–	–	10	–	0.01	10	–	–	140	μA
		10	–	–	2	–	0.005	2	–	–	120	–	–	20	–	0.02	20	–	–	280	
Quiescent Device Dissipation/Package (P_D)		5	–	–	5	–	0.025	5	–	–	300	–	–	50	–	0.05	50	–	–	700	μW
		10	–	–	20	–	0.05	20	–	–	1200	–	–	200	–	0.2	200	–	–	2800	
Output Voltage: Low-Level (V_{OL})	V_{IN} = 5	5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
	V_{IN} = 10	10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	
High-Level (V_{OH})	V_{IN} = 0	5	4.99	–	–	4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
	V_{IN} = 0	10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NL})	V_O > 3.5	5	1.5	–	–	1.5	2.25	–	1.4	–	–	1.5	–	–	1.5	2.25	–	1.4	–	–	V
	V_O > 7.0	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	V_O < 1.5	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	V_O < 3.0	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current: N-Channel (I_DN)	V_O = 0.5	5	0.65	–	–	0.5	1	–	0.35	–	–	0.35	–	–	0.3	1	–	0.24	–	–	mA
	V_O = 0.5	10	1.25	–	–	1.0	2.5	–	0.75	–	–	0.72	–	–	0.6	2.5	–	0.5	–	–	
P-Channel (I_DP)	V_O = 4.5	5	−0.31	–	–	−0.25	−0.5	–	−0.175	–	–	−0.17	–	–	−0.14	−0.5	–	−0.095	–	–	mA
	V_O = 9.5	10	−0.8	–	–	−0.65	−1.3	–	−0.45	–	–	−0.4	–	–	−0.33	−1.3	–	−0.27	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

Note 1: Devices should not be connected with power on.

*Test performed with the following sequence of 1's and 0's.

C_L	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

dynamic electrical characteristics at T_A = 25°C and C_L = 15 pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

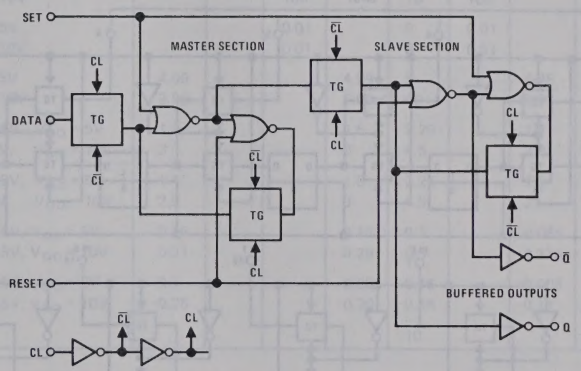
CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			MM4613AD, MM4613AF			MM5613AN			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
CLOCKED OPERATION									
Propagation Delay Time: (t_{PHL} = t_{PLH})		5	–	150	250	–	150	250	ns
		10	–	75	110	–	75	125	
Transition Time (t_{THL} = t_{TLH})		5	–	75	125	–	75	150	ns
		10	–	50	70	–	50	75	
Minimum Clock Pulse Width (t_{WL} = t_{WH})		5	–	125	175	–	125	200	ns
		10	–	50	80	–	50	100	
Maximum Clock Rise & Fall Time (*t_{rCL} = t_{fCL})		5	15	–	–	15	–	–	μs
		10	5	–	–	5	–	–	
Set-Up Time		5	–	20	40	–	20	50	ns
		10	–	10	20	–	10	25	
Maximum Clock Frequency (f_{CL})		5	3	4	–	2.5	4	–	MHz
		10	7	10	–	5	10	–	
Input Capacitance (C_I)	Any Input		–	5	–	–	5	–	pF
SET & RESET OPERATION									
Propagation Delay Time: ($t_{PHL(R)}$) ($t_{PLH(S)}$)		5	–	175	225	–	175	250	ns
		10	–	75	110	–	75	125	
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$, $t_{WH(R)}$)		5	–	125	175	–	125	200	ns
		10	–	50	80	–	50	100	

truth table

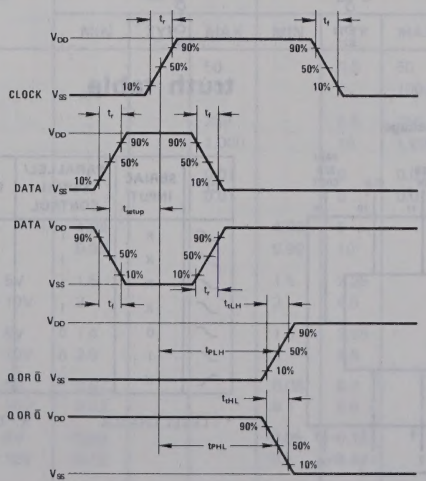
CL†	D	R	S	Q	$\bar{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	*	*

No change
* = Invalid condition
** = FF1/FF2 terminal assignments
† = Level change
x = Don't care case

logic diagram



switching time waveforms



MM4614A/MM5614A 8-stage static shift register

general description

The MM4614A/MM5614A is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

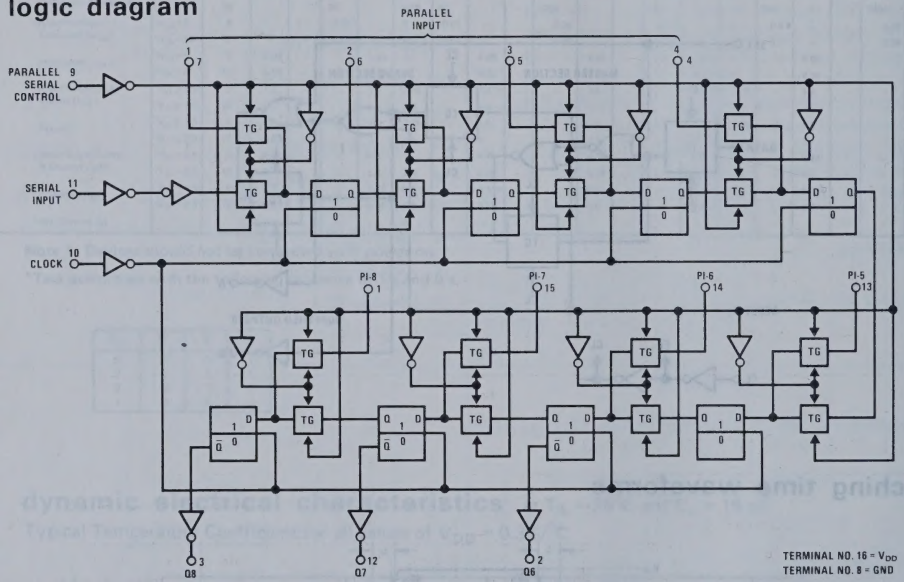
features

- Synchronous operation
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Medium speed operation — 5 MHz typ
  clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation
- Low power

applications

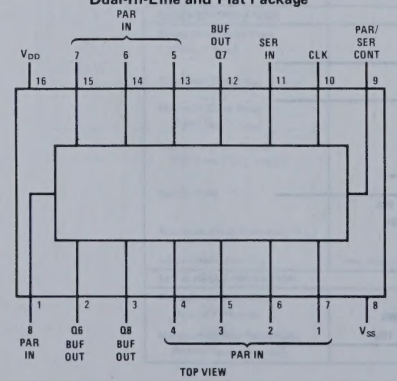
- Parallel to serial conversion
- General purpose register

logic diagram



connection diagram

Dual-In-Line and Flat Package



truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
⌐¯	X	1	0	0	0	0	
⌐¯	X	1	1	0	1	0	
⌐¯	X	1	0	1	0	1	
⌐¯	X	1	1	1	1	1	
⌐¯	0	0	X	X	0	$Q_{n\,1}$	
⌐¯	1	0	X	X	1	$Q_{n\,1}$	
¯⌐	X	X	X	X	Q1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
MM4614A	−55°C to +125°C
MM5614A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4614AD, MM4614AF

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	μA
	V_{DD} = 10V			10		1	10			600	μA
Quiescent Device Dissipation	V_{DD} = 5V			25		2.5	25			1,500	μW
Package (P_D)	V_{DD} = 10V			100		10	100			6,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.1			−0.08	−0.16		−0.055			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5614AN

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1,400	μA
Quiescent Device Dissipation	V_{DD} = 5V			250		2.5	250			3,500	μW
Package (P_D)	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.06			−0.05	−0.16		−0.04			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

dynamic electrical characteristics MM4614AD, MM4614AF

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	350	ns
	V_{DD} = 10V		50	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	2.5		MHz
	V_{DD} = 10V	3	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

dynamic electrical characteristics MM5614AN

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	1,000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	2.5		MHz
	V_{DD} = 10V	2.5	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

MM4616A/MM5616A quad bilateral switch

general description

The MM4616A/MM5616A is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

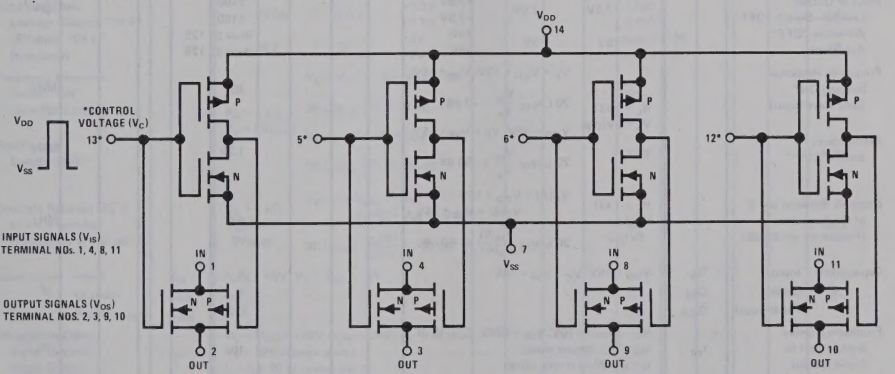
features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ.
■ Wide range of digital and analog levels	±7.5 V_{PEAK}
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS} = 15V$
■ Matched switch characteristics	$\Delta R_{ON} = 40\Omega$ typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ $f_{is} = 10$ kHz $R_L = 10k$
■ High degree of linearity	.5% distortion typ. @ $f_{is} = 1$ kHz
■ Extremely low leakage	$V_{is} = 5\ V_{p-p}$ $V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$
■ Transmits frequencies up to 10 MHz	

applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

schematic and connection diagrams

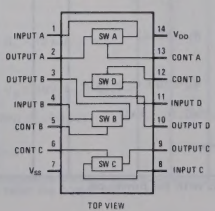


Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{IS} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}

Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1) V_{SS} −0.3V to V_{SS} +15.5V
Operating Temperature Range MM4616A −55°C to +125°C
MM5616A −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Lead Temperature (Soldering, 10 sec) 300°C
Operating V_{DD} Range V_{SS} +3V to V_{SS} +15V

electrical characteristics (MM4616AD)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −55°C MIN	−55°C TYP	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C TYP	125°C MAX	UNITS
Quiescent Dissipation per Package	P_T	TERMINALS: V_{DD} 14 @ +10 VOLTS APPLIED; V_{SS} 7 @ GND; V_C 5, 6, 12, 13 @ GND; V_{is} 1, 4, 8, 11 @ ≤ +10; V_{os} 2, 3, 9, 10 @ ≤ +10										
All Switches "OFF"					5		0.1	5			300	μW
All Switches "ON"		TERMINALS: V_{DD} 14 @ +10 VOLTS APPLIED; V_{SS} 7 @ GND; V_C 5, 6, 12, 13 @ +10; $V_{is} = V_{OS}$ 1-4, 8-11 @ ≤ +10			5		0.1	5			300	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = −10 μA, V_{DD} = 5V, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_{is}: +7.5V		120	360		200	400		300	600	
		+7.5V, −7.5V, −7.5V		120	360		200	400		300	600	Ω
		±0.25V		130	775		280	850		470	1230	
		+5V		130	600		250	660		400	960	
		+5V, −5V, −5V		130	600		250	660		400	960	Ω
		±0.25V		325	1870		580	2000		900	2600	
		+15V		120	360		200	400		300	600	
		+15V, 0V, +0.25V		120	360		200	400		300	600	Ω
		9.3V		150	775		300	850		490	1230	
		+10V		130	600		250	660		400	960	
		+10V, 0V, +0.25V		130	600		250	660		400	960	Ω
		5.6V		300	1870		560	2000		880	2600	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, −7.5V, ±7.5V					10					Ω
		+5V, −5V, ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		V_{DD} / $V_C = V_{SS}$ / V_{is}: +7.5V / −7.5V / +7.5V					±100					pA
		+7.5V / −7.5V / −7.5V					±100					
		+5V / −5V / +5V					(Note 2)	125				nA
		+5V / −5V / −5V					(Note 2)	125				
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V; R_L = 1 kΩ, V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		R_L = 1 kΩ, V_{is}(A) = 5V(p-p); V_C(A) = V_{DD} = +5V, V_C(B) = V_{SS} = −5V; $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					pF
Output	C_{OS}						4					
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF; V_{is} = 10V (square wave); $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave); R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns; $V_{is} \leq$ 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.
Note 2: $\pm 10 \times 10^{-3}$.
Note 3: Symmetrical about 0V.

electrical characteristics (MM5616AN)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS -40°C MIN	-40°C TYP	-40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C TYP	85°C MAX	UNITS
Quiescent Dissipation per Package												
		TERMINALS / VOLTS APPLIED										
		V_{DD} 14 +10										
All Switches "OFF"		V_{SS} 7 GND			5		0.1	5			80	μW
		V_C 5, 6, 12, 13 GND										
		V_{is} 1, 4, 8, 11 ≤ +10										
	P_T	V_{os} 2, 3, 9, 10 ≤ +10										
		TERMINALS / VOLTS APPLIED										
		V_{DD} 14 +10										
All Switches "ON"		V_{SS} 7 GND			5		0.1	5			80	μW
		V_C 5, 6, 12, 13 +10										
		$V_{is} = V_{OS}$ 1-4, 8-11 ≤ +10										
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		-1.7			-1.5			-1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
		$V_C = V_{DD}$ V_{SS} V_{is}										
		+7.5V -7.5V +7.5V		130	370		200	400		260	520	
		+7.5V -7.5V -7.5V		130	370		200	400		260	520	Ω
		+7.5V -7.5V ±0.25V		160	790		280	850		400	1080	
		+5V -5V +5V		150	610		250	660		340	840	
		+5V -5V -5V		150	610		250	660		340	840	Ω
"ON" Resistance	R_{ON}	R_L = 10kΩ, +7.5V -7.5V ±0.25V		370	1900		580	2000		770	2380	
		+7.5V -7.5V +15V		130	370		200	400		260	520	
		+15V 0V +0.25V		130	370		200	400		260	520	Ω
		+15V 0V 9.3V		180	790		300	850		400	1080	
		+10V 0V +10V		150	610		250	660		340	840	
		+10V 0V +0.25V		150	610		250	660		340	2380	Ω
		+10V 0V 5.6V		350	1900		560	2000		750	2380	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V -7.5V ±7.5V					10					Ω
		+5V -5V ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz, +5V -5V 5V(p-p) (Note 3)					0.4					%
		V_{DD} $V_C = V_{SS}$ V_{is}										
Input or Output Leakage–Switch "OFF" (Effective "OFF" Resistance)		+7.5V -7.5V +7.5V					±100					pA
		+7.5V -7.5V -7.5V					±100					
		+5V -5V +5V					(Note 2)	125				nA
		+5V -5V -5V					(Note 2)	125				
Frequency Response–Switch "ON" (Sine Wave Input)		$V_C = V_{DD} = +5V$, $V_{SS} = -5V$; R_L = 1 kΩ, V_{is} = 5V(p-p); 20 $\text{Log}_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		$V_{DD} = +5V$, $V_C = V_{SS} = -5V$; 20 $\text{Log}_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at –50 dB)		$V_C(A) = V_{DD} = +5V$, $V_C(B) = V_{SS} = -5V$; R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p); 20 $\text{Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = –5V					4					
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V$, V_{SS} = GND, C_L = 15 pF, V_{is} = 10V (square wave), $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS}$ = 15V, 10V, 5V, I_{IS} = 10 μA				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ, V_C = 10V (square wave)					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns, V_{is} < 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.
Note 2: $\pm 10 \times 10^{-3}$.
Note 3: Symmetrical about 0V.

typical ON resistance characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: $R_{ON} = 0\Omega$.

MM4617A/MM5617A divide-by-10 counter/divider with 10 decoded outputs

general description

The MM4617A/MM5617A is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit. The counter is cleared to its zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the MM4617A/MM5617A permits medium speed operation and assures a hazard free counting sequence. The 10 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10 clock input cycles and is used as a ripple carry signal to any succeeding stages.

features

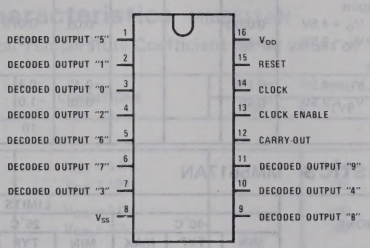
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

applications

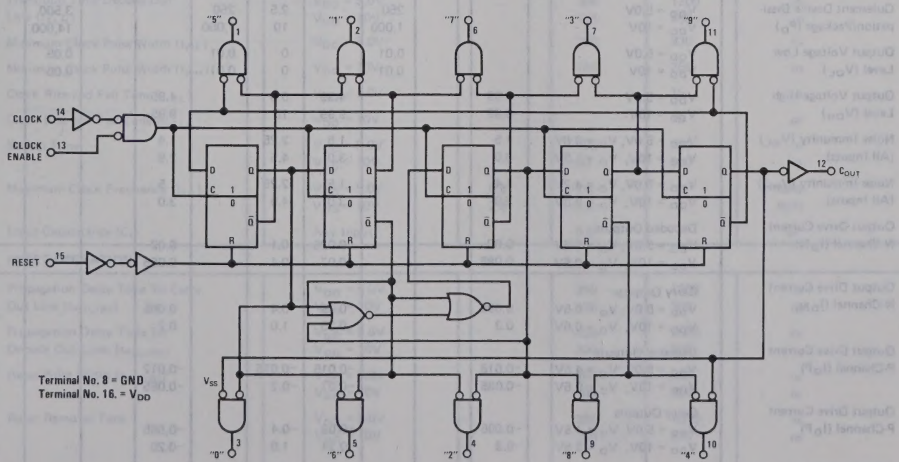
- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

connection and logic diagrams

Dual-In-Line and Flat Package



TOP VIEW



Terminal No. 8 = GND
Terminal No. 16. = V_{DD}

absolute maximum ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM4617A	−55°C to +125°C
MM5617A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics MM4617AD, MM4617AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	µA
	V_{DD} = 10V			10		0.5	10			600	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	µW
	V_{DD} = 10V			100		5.0	100			6,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.06			0.05	0.1		0.035			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.4		0.07			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.185			0.15	0.4		0.105			mA
	V_{DD} = 10V, V_O = 0.5V	0.45			0.35	1.0		0.25			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.0375			−0.03	−0.075		−0.021			mA
	V_{DD} = 10V, V_O = 9.5V	−0.12			−0.1	−0.2		−0.07			mA
Output Drive Current P-Channel (I_DP)	Carry Output										
	V_{DD} = 5.0V, V_O = 4.5V	−0.185			−0.15	−0.4		−0.105			mA
	V_{DD} = 10V, V_O = 9.5V	−0.45			−0.35	−1.0		−0.25			mA
Input Current (I_I)						10					pA

electrical characteristics MM5617AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1.0	100			1,400	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			250		2.5	250			3,500	µW
	V_{DD} = 10V			1,000		10	1,000			14,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.03			0.025	0.1		0.02			mA
	V_{DD} = 10V, V_O = 0.5V	0.085			0.07	0.4		0.055			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.095			0.08	0.4		0.065			mA
	V_{DD} = 10V, V_O = 0.5V	0.3			0.25	1.0		0.2			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.018			−0.015	−0.075		−0.012			mA
	V_{DD} = 10V, V_O = 9.5V	−0.085			−0.07	−0.2		−0.055			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.095			−0.08	−0.4		−0.065			mA
	V_{DD} = 10V, V_O = 9.5V	−0.3			−0.24	1.0		−0.20			mA
Input Current (I_I)						10					pA

dynamic electrical characteristics MM4617AD, MM4617AF

$T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

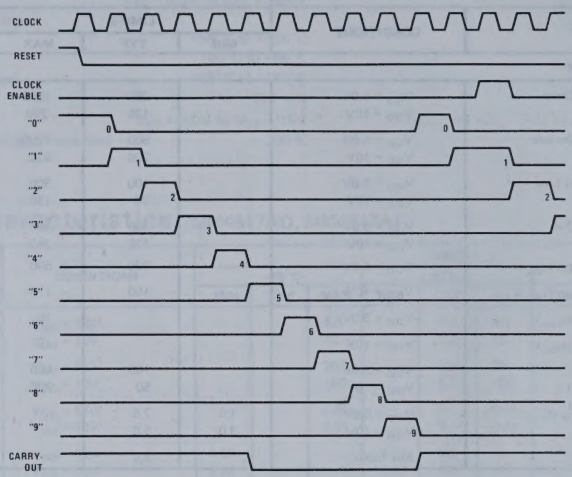
PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	$V_{DD} = 5.0V$		350	1000	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time Decode Out Lines (t_{PLH})	$V_{DD} = 5.0V$		500	1200	ns
	$V_{DD} = 10V$		200	400	ns
Transition Time Carry-Out Line (t_{THL})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		50	150	ns
Transition Time Decode-Out Line (t_{TLH})	$V_{DD} = 5.0V$		300	900	ns
	$V_{DD} = 10V$		125	350	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		100	170	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	μs
Set-Up Time	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	200	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	2.5		MHz
	$V_{DD} = 10V$	3.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time To Carry Out Line ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	1000	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time To Decode Out Lines ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		450	1200	ns
	$V_{DD} = 10V$		200	400	ns
Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		200	500	ns
	$V_{DD} = 10V$		100	165	ns
Reset Removal Time	$V_{DD} = 5.0V$		300	750	ns
	$V_{DD} = 10V$		100	225	ns

dynamic electrical characteristics MM5617AN

$T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	$V_{DD} = 5.0V$		350	1300	ns
	$V_{DD} = 10V$		125	300	ns
Propagation Delay Time Decode Out Lines (t_{PLH})	$V_{DD} = 5.0V$		500	1600	ns
	$V_{DD} = 10V$		200	500	ns
Transition Time Carry-Out Line (t_{THL})	$V_{DD} = 5.0V$		100	350	ns
	$V_{DD} = 10V$		50	200	ns
Transition Time Decode-Out Line (t_{TLH})	$V_{DD} = 5.0V$		300	1200	ns
	$V_{DD} = 10V$		125	450	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		200	830	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		100	250	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	μs
Set-Up Time	$V_{DD} = 5.0V$		100	700	ns
	$V_{DD} = 10V$		50	300	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	0.6	2.5		MHz
	$V_{DD} = 10V$	2.5	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time To Carry Out Line ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	1300	ns
	$V_{DD} = 10V$		125	300	ns
Propagation Delay Time To Decode Out Lines ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		450	1600	ns
	$V_{DD} = 10V$		200	500	ns
Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		200	830	ns
	$V_{DD} = 10V$		100	250	ns
Reset Removal Time	$V_{DD} = 5.0V$		300	1000	ns
	$V_{DD} = 10V$		100	275	ns

switching time waveforms



MM4619A/MM5619A quad AND-OR select gate

general description

The MM4619A/MM5619A is a Complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N AND P-channel enhancement mode transistors. These Complementary MOS (CMOS) transistors provide the building blocks for the four "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

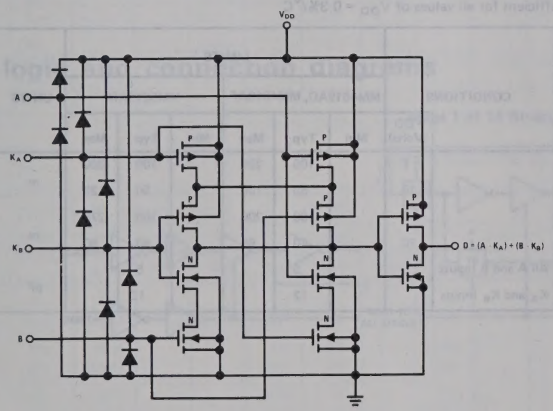
features

- Wide Supply Voltage Range — 3V to 15V
- High Noise Immunity — $0.45V_{CC}$ typ.
- Medium-Speed Operation — $t_{PHL} = t_{PLH}$ = 50 ms typ at 15 pF

applications

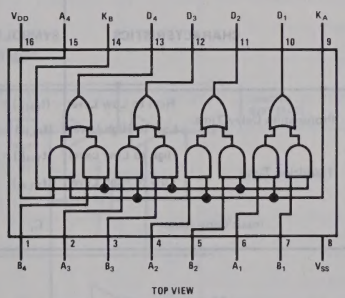
- AND-OR Select Gating
- Shift-Right/Shift-Left Registers
- True/Complement Selection
- AND/OR/EXCLUSIVE-OR Selection

schematic and connection diagrams



Schematic diagram for 1 of 4 identical stages.

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Voltage at any pin (Note 1)	V_{SS} −0.3V to V_{SS} +15.5V	Package dissipation	500 mW
Operating temperature range MM4619A	−55°C to +125°C	Lead temperature (soldering, 10 sec)	300°C
MM5619A	−40°C to +85°C	Operating V_{DD} range	V_{SS} +3V to V_{SS} +15V
Storage temperature range	−65°C to +150°C		

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

static electrical characteristics

CHARACTERISTIC	SYMBOL	CONDITIONS			LIMITS																UNITS
					MM4619AD, MM4619AF									MM5619AN							
			V_O	V_{DD}	−55°C			25°C			125°C			−40°C			25°C			85°C		
			Volts	Volts	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Quiescent Device Current	I_L			5			5		0.03	5			300			50		0.1	50			700	μA
				10			10		0.05	10			600			100		0.2	100			1400	
Quiescent Device Dissipation/Package	P_D			5			25		0.15	25			1500			250		0.5	250			3500	μW
				10			100		0.5	100			6000			1000		2	1000			14000	
Output Voltage Low Level	V_{OL}			5			0.01		0	0.01			0.05			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05			0.01		0	0.01			0.05	
High Level	V_{OH}			5	4.99			4.99	5		4.95			4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			9.99			9.99	10		9.95			
Threshold Voltage N-Channel	$V_{TH}N$	I_D = 20 μA				1.7			1.5			1.3			1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_D = −20 μA				−1.7			−1.5			−1.3			−1.7			−1.5			−1.3		V
Noise Immunity (All Inputs)	V_{NL}		0.95	5	1.5			1.5	2.25		1.4			1.5			1.5	2.25		1.4			V
			2.9	10	3			3	4.5		2.9			3			3	4.5		2.9			
	V_{NH}		3.6	5	1.4			1.5	2.25		1.5			1.4			1.5	2.25		1.5			V
			7.2	10	2.9			3	4.5		3			2.9			3	4.5		3			
Output Drive Current N-Channel	I_DN		0.5	5	0.6			0.45	1.5		0.30			0.37			0.30	1.0		0.23			mA
			0.5	10	0.9			0.75	2.5		0.55			0.8			0.65	1.5		0.6			
P-Channel	I_DP		4.5	5	−0.31			−0.25	−0.5		−0.175			−0.145			−0.12	−0.5		−0.095			mA
			9.5	10	−0.95			−0.7	−1.5		−0.5			−0.6			−0.5	−1.5		−0.4			
Input Current	I_I								10									10					pA

dynamic electrical characteristics

T_A = 25°C and C_L = 15 pF Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS		SYMBOLS	CONDITIONS	LIMITS						UNITS
				MM4619AD, MM4619AF			MM5619AN			
			V_{DD} (Volts)	Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time:	High to Low Level	(t_{PHL}) =	5		100	225		100	300	ns
	Low to High Level	(t_{PLH})	10		50	100		50	125	
Transition Time	High to Low Level	(t_{THL}) =	5		100	200		100	275	ns
	Low to High Level	(t_{TLH})	10		40	65		40	80	
Input Capacitance		C_I	All A and B Inputs		5			5		pF
			K_A and K_B Inputs		12			12		

MM4620A/MM5620A
14-stage ripple-carry binary counter/divider

general description

The MM4620A/MM5620A is a 14-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

features

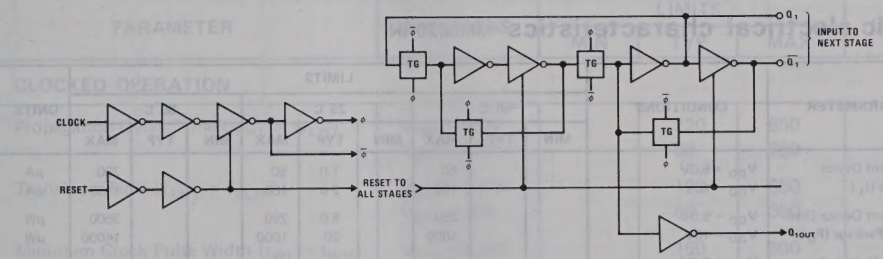
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Medium speed operation	7.0 MHz typ with V_{DD} = 10V
■ Low power	
■ Fully static operation	

applications

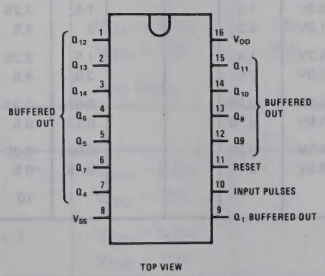
- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

logic and connection diagrams

Stage 1 of 14 Binary Stages



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 15.5$
Operating Temperature Range	
MM4620A	$-55^{\circ}C$ to $+125^{\circ}C$
MM5620A	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

static electrical characteristics MM4620AD, MM4620AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		$-55^{\circ}C$			$25^{\circ}C$			$125^{\circ}C$			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5.0V$			15		0.5	15			900	μA
	$V_{DD} = 10V$			25		1.0	25			1500	μA
Quiescent Device Dissipation Package (P_D)	$V_{DD} = 5.0V$			75		2.5	75			4500	μW
	$V_{DD} = 10V$			250		10	250			15000	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5.0V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5.0V$	4.99			4.99	5.0		4.95			V
	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.8V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 1.0V$	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5.0V$, $V_O = 4.2V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 9.0V$	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5.0V$, $V_O = 0.5V$	0.9			0.075	0.2		0.05			mA
	$V_{DD} = 10V$, $V_O = 0.5V$	0.185			0.15	0.4		0.105			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5.0V$, $V_O = 4.5V$	−0.11			−0.09	−0.25		−0.065			mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−0.25			−0.20	−0.5		−0.14			mA
Input Current (I_I)	Any Input					10					pA

static electrical characteristics MM5620AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5.0V$			50		1.0	50			700	μA
	$V_{DD} = 10V$			100		2.0	100			1400	μA
Quiescent Device Dissipation Package (P_D)	$V_{DD} = 5.0V$			250		5.0	250			3500	μW
	$V_{DD} = 10V$			1000		20	1000			14000	μW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5.0V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5.0V$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.8V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$, $V_O = 1.0V$	3.0			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5.0V$, $V_O = 4.2V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$, $V_O = 9.0V$	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5.0V$, $V_O = 0.5V$	0.85			0.07	0.33		0.60			mA
	$V_{DD} = 10V$, $V_O = 0.5V$	0.16			0.13	0.5		0.10			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5.0V$, $V_O = 4.5V$	−0.09			−0.06	−0.25		−0.05			mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−0.18			−0.15	−0.5		−0.12			mA
Input Current (I_I)	Any Input					10					pA

dynamic electrical characteristics MM4620AD, MM4620AF

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL} Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		220	600	ns
	$V_{DD} = 10V$		80	225	ns
Transition Time ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		120	600	ns
	$V_{DD} = 10V$		60	300	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$		150	335	ns
	$V_{DD} = 10V$		50	125	ns
Clock Rise and Fall Time ($t_{rCL} = t_{fCL}$)	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			15	μs
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.5	3.0		MHz
	$V_{DD} = 10V$	4.0	10		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	3000	ns
	$V_{DD} = 10V$		150	775	ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		350	2500	ns
	$V_{DD} = 10V$		150	475	ns

dynamic electrical characteristics MM5620AN

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL} Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		220	650	ns
	$V_{DD} = 10V$		80	250	ns
Transition Time ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		120	650	ns
	$V_{DD} = 10V$		60	350	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$		150	500	ns
	$V_{DD} = 10V$		50	165	ns
Clock Rise and Fall Time ($t_{rCL} = t_{fCL}$)	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			15	μs
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	3.0		MHz
	$V_{DD} = 10V$	3.0	10		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	3500	ns
	$V_{DD} = 10V$		150	900	ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		350	3000	ns
	$V_{DD} = 10V$		150	550	ns

MM4621A/MM5621A 8-stage static shift register

general description

The MM4621A/MM5621A is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is "jammed" into each stage of the register asynchronously with the clock.

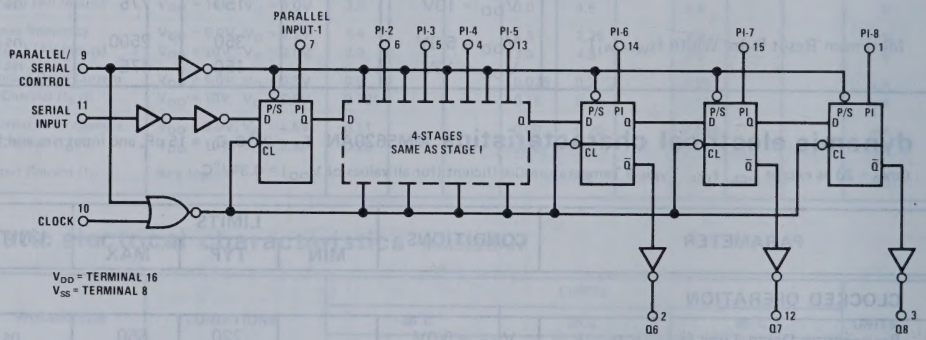
features

- Asynchronous parallel or synchronous serial operation.
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Medium speed operation — 5 MHz typ
  clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation

applications

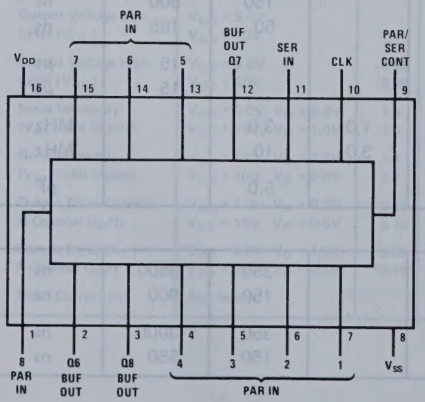
- Parallel to serial data conversion
- General purpose register

logic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n
X	X	1	Q	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⌐	0	0	X	X	0	Q_n 1
⌐	1	0	X	X	1	Q_n 1
⌐	X	0	X	X	Q1	Q_n

NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
MM4621A	−55°C to +125°C
MM5621A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4621AD, MM4621AF

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	μA
	V_{DD} = 10V			10		1	10			600	μA
Quiescent Device Dissipation	V_{DD} = 5V			25		2.5	25			1,500	μW
Package (P_D)	V_{DD} = 10V			100		10	100			6,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.1			−0.08	−0.16		−0.055			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5621AN

PARAMETERS	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1,400	μA
Quiescent Device Dissipation	V_{DD} = 5V			250		2.5	250			3,500	μW
Package (P_D)	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.06			−0.05	−0.16		−0.04			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

dynamic electrical characteristics MM4621AD, MM4621AF

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	350	ns
	V_{DD} = 10V		50	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	2.5		MHz
	V_{DD} = 10V	3	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

dynamic electrical characteristics MM5621AN

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	1,000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	2.5		MHz
	V_{DD} = 10V	2.5	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

MM4622A/MM5622A divide-by-8 counter/divider with 8 decoded outputs

general description

The MM4622A/MM5622A is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit. The counter is cleared to its zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the MM4622A/MM5622A permits medium speed operation and assures an error free counting sequence. The 8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

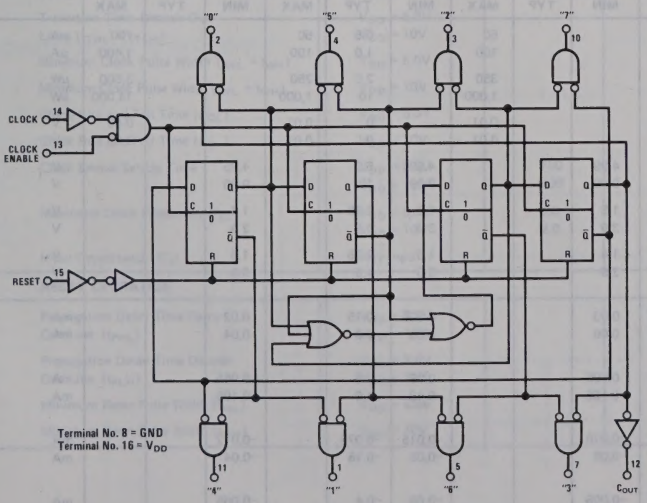
features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

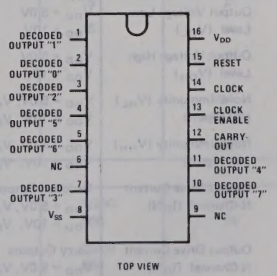
applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM4622A	−55°C to +125°C
MM5622A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics MM4622AD, MM4622AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	μA
	V_{DD} = 10V			10		0.5	10			600	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	μW
	V_{DD} = 10V			100		5.0	100			6,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.062			0.05	0.15		0.035			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.3		0.07			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.185			0.15	0.5		0.105			mA
	V_{DD} = 10V, V_O = 0.5V	0.375			0.3	1.0		0.21			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.038			−0.03	−0.075		−0.021			mA
	V_{DD} = 10V, V_O = 9.5V	−0.062			−0.05	−0.15		−0.035			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.185			−0.15	−0.4		−0.105			mA
	V_{DD} = 10V, V_O = 9.5V	−0.375			−0.3	−0.8		−0.21			mA
Input Current (I_I)						10					pA

electrical characteristics MM5622AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1.0	100			1,400	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			350		2.5	250			3,500	μW
	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.03			0.025	0.15		0.02			mA
	V_{DD} = 10V, V_O = 0.5V	0.06			0.05	0.3		0.04			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.095			0.08	0.5		0.065			mA
	V_{DD} = 10V, V_O = 0.5V	0.155			0.13	1.0		0.105			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.018			−0.015	−0.075		−0.012			mA
	V_{DD} = 10V, V_O = 9.5V	−0.06			−0.05	−0.15		−0.04			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.095			−0.08	−0.4		−0.065			mA
	V_{DD} = 10V, V_O = 9.5V	−0.155			−0.13	−0.8		−0.105			mA
Input Current (I_I)						10					pA

dynamic electrical characteristics MM4622AD, MM4622AF

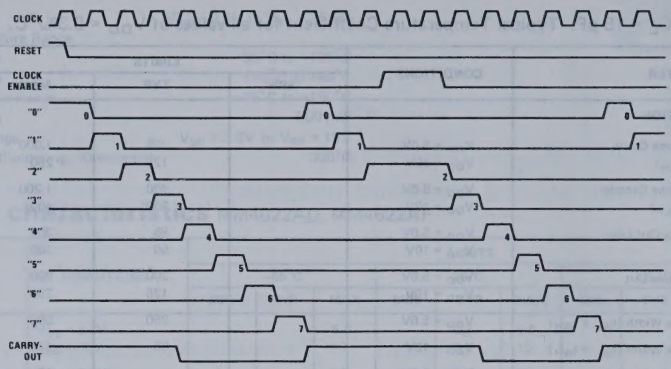
$T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		325	1,000	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time Decode-Out Lines ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		400	1,200	ns
	$V_{DD} = 10V$		200	400	ns
Transition Time Carry-Out Line ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		85	300	ns
	$V_{DD} = 10V$		50	100	ns
Transition Time Decode-Out Lines ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		300	900	ns
	$V_{DD} = 10V$		125	250	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$		250	500	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 10V$		85	170	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	μs
Clock Enable Set-Up Time	$V_{DD} = 5.0V$	350	175		ns
	$V_{DD} = 10V$	150	75		ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	2.5		MHz
	$V_{DD} = 10V$	3.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time Carry-Out Line (t_{PLH})	$V_{DD} = 5.0V$		300	900	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time Decode-Out Line (t_{PLH})	$V_{DD} = 5.0V$		500	1,250	ns
	$V_{DD} = 10V$		200	400	ns
Minimum Reset Pulse Width (t_{WL})	$V_{DD} = 5.0V$		150	300	ns
Minimum Reset Pulse Width (t_{WH})	$V_{DD} = 10V$		75	150	ns

dynamic electrical characteristics MM5622AN

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		325	1,300	ns
	$V_{DD} = 10V$		125	500	ns
Propagation Delay Time Decode-Out Line ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$		400	1,600	ns
	$V_{DD} = 10V$		200	800	ns
Transition Time Carry-Out Line ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		85	340	ns
	$V_{DD} = 10V$		50	200	ns
Transition Time Decode-Out Lines ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$		300	1,200	ns
	$V_{DD} = 10V$		125	500	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$		250	830	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 10V$		85	250	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	μs
Clock Enable Set-Up Time	$V_{DD} = 5.0V$	700	175		ns
	$V_{DD} = 10V$	300	75		ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	0.6	2.5		MHz
	$V_{DD} = 10V$	2.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	$V_{DD} = 5.0V$		300	1,200	ns
	$V_{DD} = 10V$		125	500	ns
Propagation Delay Time Decode-Out Line (t_{PLH})	$V_{DD} = 5.0V$		500	2,500	ns
	$V_{DD} = 10V$		200	800	ns
Minimum Reset Pulse Width (t_{WL})	$V_{DD} = 5.0V$		150	600	ns
Minimum Reset Pulse Width (t_{WH})	$V_{DD} = 10V$		75	300	ns

timing diagram



MM4624A/MM5624A 7-stage ripple-carry binary counter/divider

general description

The MM4624A/MM5624A is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

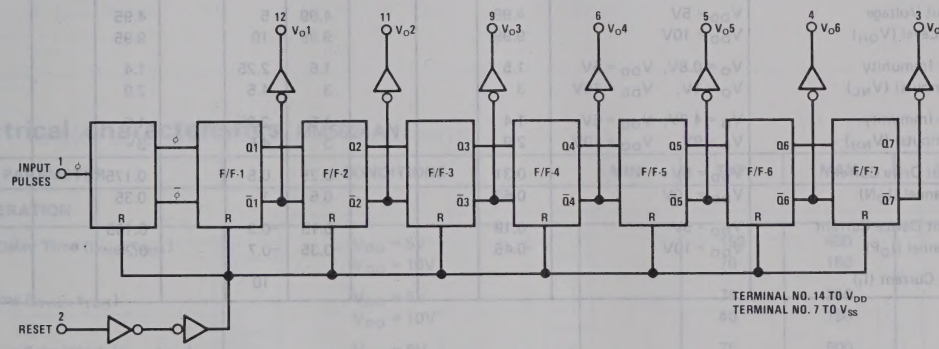
features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ High speed	12 MHz (typ) input pulse rate $V_{DD}-V_{SS}$ = 10V
■ Fully static operation	
■ Low power	

applications

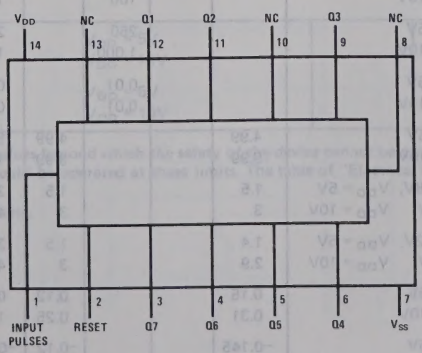
- Frequency dividing circuits
- Time-delay circuits
- Counter control

logic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 15.5$
Operating Temperature Range	
MM4624A	−55°C to +125°C
MM5624A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Leading Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4624AD, MM4624AF

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			5		0.3	5			300	μA
	$V_{DD} = 10V$			10		0.5	10			600	μA
Quiescent Device Dissipation	$V_{DD} = 5V$			25		1.5	25			1,500	μW
Package (P_D)	$V_{DD} = 10V$			100		5	100			6,000	μW
Output Voltage	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage	$V_{DD} = 5V$	4.99			4.99	5		4.95			V
High-Level (V_{OH})	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity	$V_O = 0.8V$, $V_{DD} = 5V$	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	$V_O = 1V$, $V_{DD} = 10V$	3			3	4.5		2.9			V
Noise Immunity	$V_O = 4.2V$, $V_{DD} = 5V$	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	$V_O = 9V$, $V_{DD} = 10V$	2.9			3	4.5		3			V
Output Drive Current	$V_{DD} = 5V$	0.31			0.25	0.5		0.175			mA
N-Channel (I_DN)	$V_{DD} = 10V$	0.62			0.5	1		0.35			mA
Output Device Current	$V_{DD} = 5V$	−0.19			−0.15	−0.3		−0.105			mA
P-Channel (I_DP)	$V_{DD} = 10V$	−0.45			−0.35	−0.7		−0.25			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5624AN

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			50		0.5	50			700	μA
	$V_{DD} = 10V$			100		1	100			1,400	μA
Quiescent Device Dissipation	$V_{DD} = 5V$			250		2.5	250			3,500	μA
Package (P_D)	$V_{DD} = 10V$			1,000		10	1,000			14,000	μA
Output Voltage	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage	$V_{DD} = 5V$	4.99			4.99	5		4.95			V
High-Level (V_{OH})	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity	$V_O = 0.8V$, $V_{DD} = 5V$	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	$V_O = 1V$, $V_{DD} = 10V$	3			3	4.5		2.9			V
Noise Immunity	$V_O = 4.2V$, $V_{DD} = 5V$	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	$V_O = 9V$, $V_{DD} = 10V$	2.9			3	4.5		3			V
Output Drive Current	$V_{DD} = 5V$	0.15			0.12	0.5		0.95			mA
N-Channel (I_DN)	$V_{DD} = 10V$	0.31			0.25	1		0.2			mA
Output Drive Current	$V_{DD} = 5V$	−0.145			−0.12	−0.3		−0.95			mA
P-Channel (I_DP)	$V_{DD} = 10V$	−0.31			−0.25	−0.7		−0.2			mA
Input Current (I_I)						10					pA

ac electrical characteristics MM4624AD, MM4624AF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ϕ INPUT OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		150	350	ns
(Note 3)	V_{DD} = 10V		70	125	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		75	225	ns
	V_{DD} = 10V		40	125	ns
Minimum Input-Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		75	330	ns
	V_{DD} = 10V		40	125	ns
Input Pulse Time ($t_{r\phi}$, $t_{f\phi}$)	V_{DD} = 5V			15	ns
	V_{DD} = 10V			10	ns
Maximum Input Pulse Frequency ($f\phi$)	V_{DD} = 5V	1.5	5		MHz
	V_{DD} = 10V	4	12		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	700	ns
	V_{DD} = 10V		100	350	ns
Minimum Pulse Reset Width ($t_{WH(R)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	300	ns

ac electrical characteristics MM5624AN

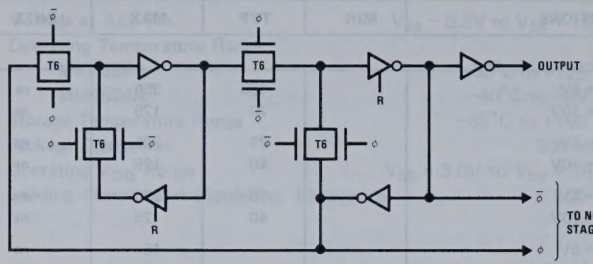
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ϕ INPUT OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		150	400	ns
(Note 3)	V_{DD} = 10V		70	150	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		75	250	ns
	V_{DD} = 10V		40	150	ns
Minimum Input-Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		75	500	ns
	V_{DD} = 10V		40	165	ns
Input Pulse Time ($t_{r\phi}$, $t_{f\phi}$)	V_{DD} = 5V			15	ns
	V_{DD} = 10V			10	ns
Maximum Input Pulse Frequency ($f\phi$)	V_{DD} = 5V	1	5		MHz
	V_{DD} = 10V	3	12		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	800	ns
	V_{DD} = 10V		100	400	ns
Minimum Pulse Reset Width ($t_{WH(R)}$)	V_{DD} = 5V		200	600	ns
	V_{DD} = 10V		100	350	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

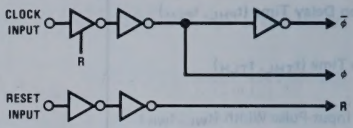
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: To Q1 output.

schematic diagram



Flip-flop logic (1 of 7 identical stages).



Input Logic

MM4625A/MM5625A triple three-input NOR gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

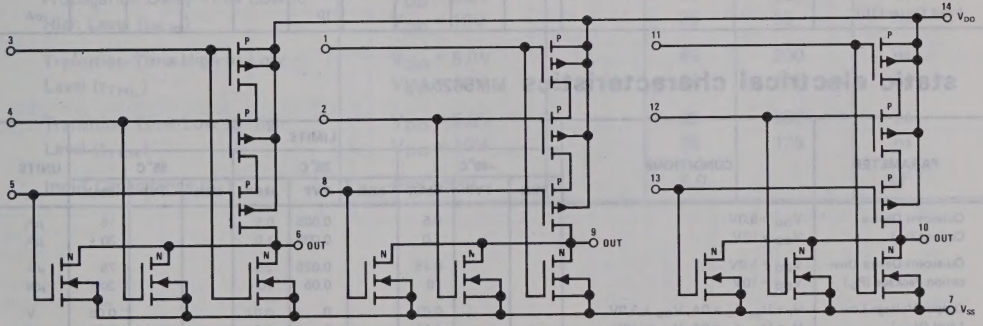
features

- Wide supply voltage range 3.0V to 15V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)
- Medium speed operation $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF

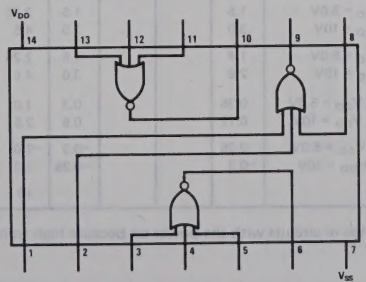
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	$V_{SS} - 0.3V$ to $V_{SS} + 15.5V$
Operating Temperature Range	
MM4625A	−55°C to +125°C
MM5625A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4625AD, MM4625AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5.0V$			0.05		0.001	0.05			3.0	μA
	$V_{DD} = 10V$			0.1		0.001	0.1			6.0	μA
Quiescent Device Dissipation Package (P_D)	$V_{DD} = 5.0V$			0.25		0.005	0.25			15	μW
	$V_{DD} = 10V$			1.0		0.01	1.0			60	μW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, $I_O = 0A$, $V_{DD} = 5.0V$			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, $I_O = 0A$, $V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, $I_O = 0A$, $V_{DD} = 5.0V$	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, $I_O = 0A$, $V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	$I_O = 0$, $V_O = 4.3V$, $V_{DD} = 5.0V$	1.5			1.5	2.25		1.4			V
	$I_O = 0$, $V_O = 9.3V$, $V_{DD} = 10V$	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	$I_O = 0$, $V_O = 0.7V$, $V_{DD} = 5.0V$	1.4			1.5	2.25		1.5			V
	$I_O = 0$, $V_O = 0.7V$, $V_{DD} = 10V$	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, $V_O = 0.4$, $V_{DD} = 5.0V$	0.5			0.40			0.28			mA
	$V_I = V_{DD}$, $V_O = 0.5$, $V_{DD} = 10V$	1.1			0.9			0.65			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq 2.5V$, $V_{DD} = 5.0V$	−0.62			−0.5			−0.35			mA
	$V_I = V_{SS}$, $V_O = 9.5V$, $V_{DD} = 10V$	−0.62			−0.5			−0.35			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5625AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5.0V$			0.5		0.005	0.5			15	μA
	$V_{DD} = 10V$			1.0		0.005	1.0			30	μA
Quiescent Device Dissipation Package (P_D)	$V_{DD} = 5.0V$			0.25		0.025	2.5			75	μA
	$V_{DD} = 10V$			10		0.05	10			300	μW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, $I_O = 0A$, $V_{DD} = 5.0V$			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, $I_O = 0A$, $V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, $I_O = 0A$, $V_{DD} = 5.0V$	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, $I_O = 0A$, $V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	$I_O = 0$, $V_O = 4.3V$, $V_{DD} = 5.0V$	1.5			1.5	2.25		1.4			V
	$I_O = 0$, $V_O = 9.3V$, $V_{DD} = 10V$	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	$I_O = 0$, $V_O = 0.7V$, $V_{DD} = 5.0V$	1.4			1.5	2.25		1.5			V
	$I_O = 0$, $V_O = 0.7V$, $V_{DD} = 10V$	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, $V_O = 0.4V$, $V_{DD} = 5.0V$	0.35			0.3	1.0		0.24			mA
	$V_I = V_{DD}$, $V_O = 0.5V$, $V_{DD} = 10V$	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq 2.5V$, $V_{DD} = 5.0V$	−0.35			−0.3	−2.0		−0.24			mA
	$V_I = V_{SS}$, $V_O = 9.5V$, $V_{DD} = 10V$	−0.3			−0.25	−1.0		−0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

dynamic eletrical characteristics MM4625AD, MM4625AF

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	70	ns
	$V_{DD} = 10V$		25	45	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
Input Capacitance (C_I)	Any Input		5.0		pF

dynamic electrical characteristics MM5625AN

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
Input Capacitance (C_I)	Any Input		5.0		pF

MM4627A/MM5627A dual JK master/slave flip-flop with set and reset

general description

These dual JK flip-flops are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

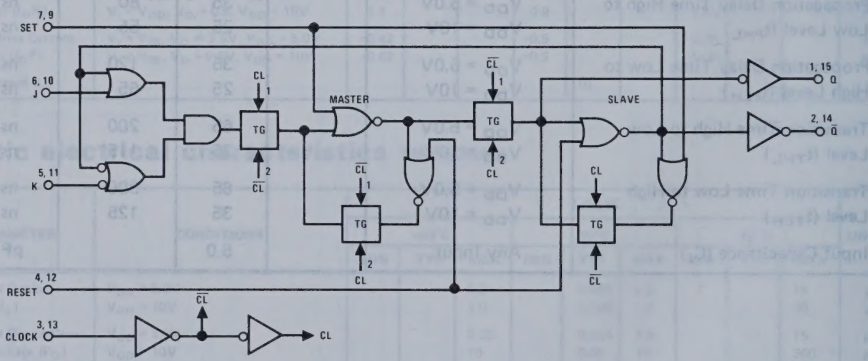
features

- Wide supply voltage range — 3.0V to 15V
- Low power — 50 nW typ
- Medium speed operation — 8.0 MHz typ with 10V supply
- High noise immunity — 0.45 V_{CC} typ

applications

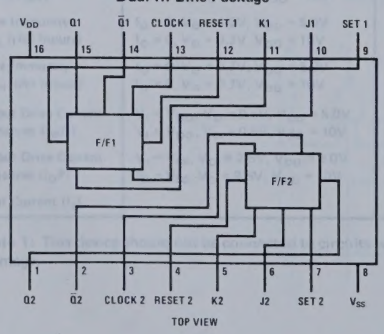
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Computers

schematic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

$*t_{n-1}$ INPUTS						$*t_n$ OUTPUTS	
CL▲	J	K	S	R	Q	Q	$\overline{Q}$
⌐	I	X	O	O	O	I	O
⌐	X	O	O	O	I	I	O
⌐	O	X	O	O	O	O	I
⌐	X	I	O	O	I	O	I
⌙	X	X	O	O	X	(No change)	
X	X	X	I	O	X	I	O
X	X	X	O	I	X	O	I
X	X	X	I	I	X	*	*

Where:

I = High Level
O = Low Level
▲ = Level Change
X = Don't Care
★ = Invalid Condition

● = t_{n-1} refers to the time interval prior to the positive clock pulse transition
♦ = t_n refers to the time intervals after the positive clock pulse transition

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM4627A	−55°C to +125°C
MM5627A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4627AD, MM4627AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			1.0		0.005	1.0			60	μA
	V_{DD} = 10V			2.0		0.005	2.0			120	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			5.0		0.025	5.0			300	μW
	V_{DD} = 10V			20		0.05	20			1,200	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.63			0.5	1.0		0.33			mA
	V_{DD} = 10V, V_O = 0.5V	1.25			1.0	2.5		0.7			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.31			−0.25	−0.5		−0.175			mA
	V_{DD} = 10V, V_O = 9.5V	−0.8			−0.65	−1.3		−0.45			mA
Input Current (I_I)	Any Input					10					pA

static electrical characteristics MM5627AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			10		0.01	10			140	μA
	V_{DD} = 10V			20		0.05	20			280	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			50		0.05	50			700	μW
	V_{DD} = 10V			200		0.02	200			2,800	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.3			0.3	1.0		0.24			mA
	V_{DD} = 10V, V_O = 0.5V	0.72			0.6	2.5		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.17			−0.14	−0.5		−0.063			mA
	V_{DD} = 10V, V_O = 9.5V	−0.4			−0.33	−1.3		−0.27			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics MM4627AD, MM4627AF

$T_A = 25°C$, $V_{SS} = 0V$, $C_L = 15$ pF, and input rise and fall times = 20 ns, except t_{rCL} and t_{fCL}.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		150	300	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		75	110	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		75	125	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	70	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		125	300	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		50	100	ns
Maximum Clock Rise and Fall Time ($^*t_{rCL}$)	$V_{DD} = 5.0V$	15			μs
Maximum Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0			μs
Set-Up Time	$V_{DD} = 5.0V$		70	150	ns
	$V_{DD} = 10V$		25	50	ns
Maximum Clock Frequency (Toggle Mode) (fCL)	$V_{DD} = 5.0V$	1.5	3.0		MHz
	$V_{DD} = 10V$	4.5	8.0		MHz
Input Capacitance (C_I)			5.0		pF
SET AND RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		175	225	ns
Propagation Delay Time ($t_{PLH(S)}$)	$V_{DD} = 10V$		75	110	ns
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$)	$V_{DD} = 5.0V$		125	200	ns
Minimum Set and Reset Pulse Widths ($t_{WL(R)}$)	$V_{DD} = 10V$		50	80	ns

dynamic electrical characteristics MM5627AN

$T_A = 25°C$, $V_{SS} = 0V$, $C_L = 15$ pF, and input rise and fall times = 20 ns, except t_{rCL} and t_{fCL}.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		150	400	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		75	150	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		75	250	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	140	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		125	400	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		50	130	ns
Maximum Clock Rise and Fall Time ($^*t_{rCL}$)	$V_{DD} = 5.0V$	15			μs
Maximum Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0			μs
Set-Up Time	$V_{DD} = 5.0V$		70	200	ns
	$V_{DD} = 10V$		25	75	ns
Maximum Clock Frequency (Toggle Mode) (fCL)	$V_{DD} = 5.0V$	1.0	3.0		MHz
	$V_{DD} = 10V$	3.0	8.0		MHz
Input Capacitance (C_I)			5.0		pF
SET AND RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		175	350	ns
Propagation Delay Time ($t_{PLH(S)}$)	$V_{DD} = 10V$		75	150	ns
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$)	$V_{DD} = 5.0V$		125	300	ns
Minimum Set and Reset Pulse Widths ($t_{WL(R)}$)	$V_{DD} = 10V$		50	120	ns

MM4630A/MM5630A quad EXCLUSIVE-OR gate

general description

These EXCLUSIVE-OR gates are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

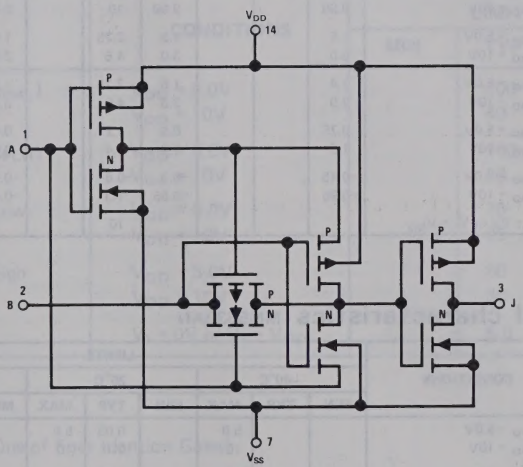
features

- Wide supply voltage range — 3.0V to 15V
- Low power — 100 nW (typ)
- Medium speed operation — $t_{PHL} = t_{PLH} = 40$ ns (typ) at $C_L = 15$ pF, 10V supply
- High noise immunity — 0.45 V_{CC} (typ)

applications

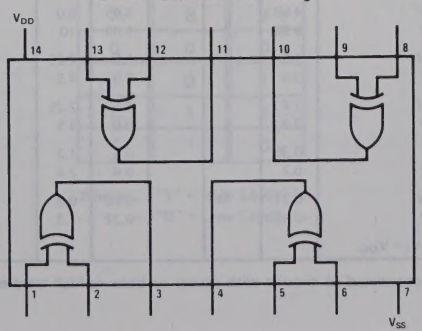
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

schematic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM4630A	−55°C to +125°C
MM5630A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4630AD, MM4630AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
	V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

static electrical characteristics MM5630AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
	V_{DD} = 10V			10		0.1	10			140	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	μW
	V_{DD} = 10V			100		1.0	100			1,400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	V_{DD} = 10V	−0.45			−0.32	−1.3		−0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics MM4630AD, MM4630AF

at $T_A = 25°C$, $V_{SS} = 0V$, and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	150	ns
	$V_{DD} = 10V$		25	75	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	150	ns
	$V_{DD} = 10V$		30	75	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

dynamic electrical characteristics MM5630AN

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	300	ns
	$V_{DD} = 10V$		25	150	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	300	ns
	$V_{DD} = 10V$		30	150	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

truth table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

MM4635A/MM5635A 4-bit parallel-in/parallel-out shift register

general description

The MM4635A/MM5635A 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. This shift register is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high."

In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high," the True contents of the register are available at the output terminals. When the True/Complement control is "low," the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

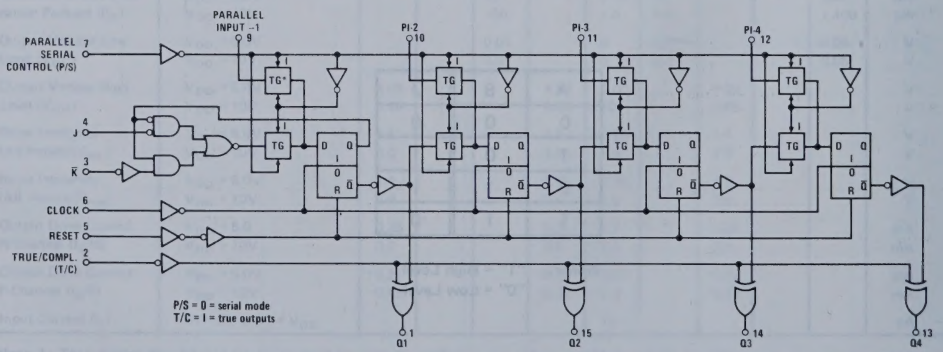
features

- Wide supply voltage range 3.0V to 15V
- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- $J\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Reset control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low-power dissipation 5.0μW typ (ceramic)
- High speed to 5.0 MHz

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

logic diagram



absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
MM46XXA	−55°C to +125°C
MM56XXA	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM4635AD, MM4635AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	μA
	V_{DD} = 10V			10		0.5	10			600	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	μW
	V_{DD} = 10V			100		5.0	100			6,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_O = 0.8V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_O = 1.0V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_O = 4.2V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_O = 9.0V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5.0V	0.62			0.50	1.0		0.35			mA
	V_O = 0.5V, V_{DD} = 10V	1.55			1.25	2.5		0.87			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5.0V	−0.31			−0.25	−0.5		−0.17			mA
	V_O = 9.5V, V_{DD} = 10V	−0.81			−0.65	−1.3		−0.45			mA
Input Current (I_I)						10					pA

static electrical characteristics MM5635AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1.0	100			1,400	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			250		2.5	250			3,500	μW
	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	V_O = 0.8V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_O = 1.0V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_O = 4.2V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_O = 9.0V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5.0V	0.43			0.35	1.0		0.24			mA
	V_O = 0.5V, V_{DD} = 10V	1.05			0.85	2.5		0.59			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5.0V	−0.2			−0.18	−0.5		−0.12			mA
	V_O = 9.5V, V_{DD} = 10V	−0.56			−0.45	−0.31		−0.31			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

dynamic electrical characteristics MM4635AD, MM4635AF

at $T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		250	500	ns
Propagation Delay Time (t_{PHL})	$V_{DD} = 10V$		100	200	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		100	200	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	100	ns
Minimum Clock Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	335	ns
Minimum Clock Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	165	ns
Clock Rise and Fall Time (t_{rCL})*	$V_{DD} = 5.0V$	15		15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0		5.0	μs
$J\overline{K}$ Lines Setup Time	$V_{DD} = 5.0V$		250	500	ns
	$V_{DD} = 10V$		100	200	ns
Parallel-In Lines Setup Time	$V_{DD} = 5.0V$		100	350	ns
	$V_{DD} = 10V$		50	80	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.5	2.5		MHz
	$V_{DD} = 10V$	3.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		250	500	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		100	200	ns
Minimum Reset Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	400	ns
Minimum Reset Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	175	ns

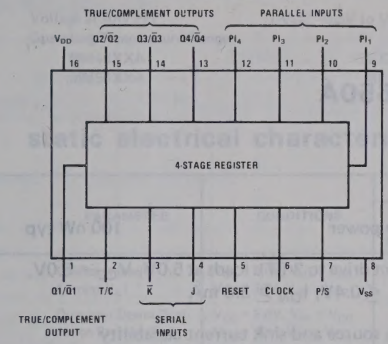
dynamic electrical characteristics MM5635AN

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		250	700	ns
Propagation Delay Time (t_{PHL})	$V_{DD} = 10V$		100	300	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		100	300	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	150	ns
Minimum Clock Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Clock Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	250	ns
Clock Rise and Fall Time (t_{rCL})*	$V_{DD} = 5.0V$	15		15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0		5.0	μs
$J\overline{K}$ Lines Setup Time	$V_{DD} = 5.0V$		250	750	ns
$J\overline{K}$ Lines Setup Time	$V_{DD} = 10V$		100	250	ns
Parallel-In Lines Setup Time	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	100	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	2.5		MHz
	$V_{DD} = 10V$	2.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		250	700	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		100	300	ns
Minimum Reset Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Reset Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	200	ns

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

connection diagram

Dual-In-Line Package



truth table

C_L	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
↓	0	X	0	0	0
↓	1	X	0	0	1
↓	X	0	0	1	0
↓	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↓	X	1	0	1	1
↑	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

MM4649A/MM5649A, MM4650A/MM5650A MOS(CMOS) hex buffers

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-Channel enhancement mode transistors. These devices feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and they can drive directly two DTL/TTL loads.

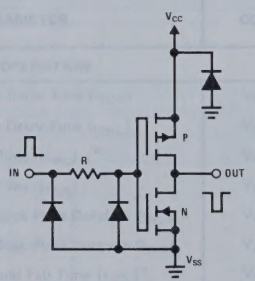
features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power — 100 nW typ
- Direct drive to 2 TTL loads at 5.0V, V_{CC} = 5.0V, $V_{OL} \leq 0.4V$, $I_{DN} \geq 3.0$ mA
- High source and sink current capability

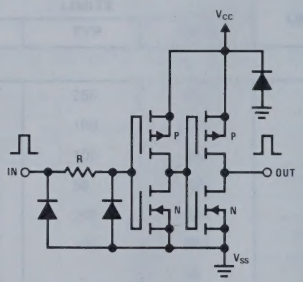
applications

- CMOS hex inverter
- CMOS to DTL/TTL hex converter
- CMOS current "Sink" or "Source" driver
- CMOS high-to-low logic-level converter

schematic diagrams



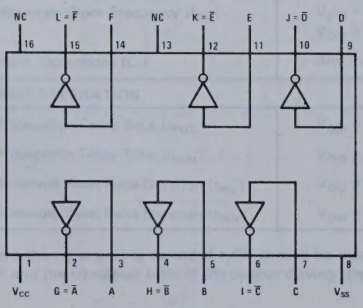
(a) Schematic Diagram of MM4649, 1 of 6 Identical Units



(b) Schematic Diagram of MM4650, 1 of 6 Identical Units

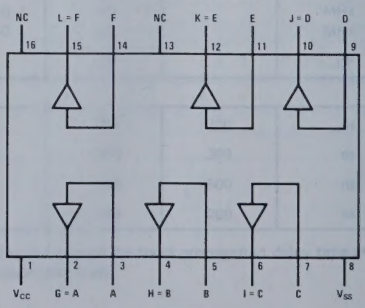
connection diagrams

Dual-In-Line and Flat Package
MM4649A/MM5649A



TOP VIEW

Dual-In-Line and Flat Package
MM4650A/MM5650A



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 15.5V	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
MM46XXA	−55°C to +125°C	Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
MM56XXA	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

static electrical characteristics MM5649AN, MM5650AN

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{CC} = 5.0V, V_{IH} = V_{CC}			3.0		0.03	3.0			42	μA
	V_{CC} = 10V, V_{IH} = V_{CC}			5.0		0.05	5.0			70	μA
Quiescent Device Dissipation Package (P_D)	V_{CC} = 5.0V, V_{IH} = V_{CC}			15		0.15	15			210	μW
	V_{CC} = 10V, V_{IH} = V_{CC}			50		0.5	50			700	μW
Output Voltage Low Level (V_{OL})	V_{CC} = 5.0V			0.01		0	0.01			0.05	V
	V_{CC} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{CC} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{CC} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs) MM4649	V_{CC} = 5.0V, V_{OH} = 3.6V	1.0			1.0	2.25		0.9			V
	V_{CC} = 10V, V_{OH} = 7.2V	2.0			2.0	4.5		1.9			V
Noise Immunity (V_{NL}) (All Inputs) MM4650	V_{CC} = 5.0V, V_{OL} = 0.95V	1.5			1.5	2.25		1.4			V
	V_{CC} = 10V, V_{OL} = 2.9V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs) MM4650	V_{CC} = 10V, V_{OH} = 7.2V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OH} = 3.6V	1.4			1.5	2.25		1.5			V
Noise Immunity (V_{NH}) (All Inputs) MM4649	V_{CC} = 10V, V_{OL} = 2.9V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OL} = 0.95V	1.4			1.5	2.25		1.5			V
Output Drive Current N-Channel (I_DN)	V_{CC} = 4.5V, V_O = 0.4V	3.1			2.6	5.2		2.1			mA
	V_{CC} = 5.0V, V_O = 0.4V	3.6			3.0	6.0		2.5			mA
	V_{CC} = 10V, V_O = 0.5V	9.6			8.0	16		6.6			mA
Output Drive Current P-Channel (I_DP)	V_{CC} = 5.0V, V_O = 4.5V	−0.6			−0.5	−1.0		−0.4			mA
	V_{CC} = 5.0V, V_O = 2.5V	−1.5			−1.25	−2.5		−1.0			mA
	V_{CC} = 10V, V_O = 9.5V	−1.5			−1.25	−2.5		−1.0			mA
Input Current (I_I)	V_{IH} = V_{CC}					10					pA

static electrical characteristics MM4649AD, MM4649AF, MM4650AD, MM4650AF

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{CC} = 5.0V, V_{IH} = V_{CC}			0.3		0.01	0.3			20	μA
	V_{CC} = 10V, V_{IH} = V_{CC}			0.5		0.01	0.5			30	μA
Quiescent Device Dissipation Package (P_D)	V_{CC} = 5.0V, V_{IH} = V_{CC}			1.5		0.05	1.5			100	μW
	V_{CC} = 10V, V_{IH} = V_{CC}			5.0		0.1	5.0			300	μW
Output Voltage Low Level (V_{OL})	V_{CC} = 5.0V			0.01		0	0.01			0.05	V
	V_{CC} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{CC} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{CC} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs) MM4649	V_{CC} = 5.0V, V_{OH} = 3.6V	1.0			1.0	2.25		0.9			V
	V_{CC} = 10V, V_{OH} = 7.2V	2.0			2.0	4.5		1.9			V
Noise Immunity (V_{NL}) (All Inputs) MM4650	V_{CC} = 5.0V, V_{OL} = 0.95V	1.5			1.5	2.25		1.4			V
	V_{CC} = 10V, V_{OL} = 2.9V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs) MM4650	V_{CC} = 10V, V_{OH} = 7.2V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OH} = 3.6V	1.4			1.5	2.25		1.5			V
Noise Immunity (V_{NH}) (All Inputs) MM4649	V_{CC} = 10V, V_{OL} = 2.9V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OL} = 0.95V	1.4			1.5	2.25		1.5			V
Output Drive Current N-Channel (I_DN)	V_{CC} = 4.5V, V_O = 0.4V	3.3			2.6	5.2		1.8			mA
	V_{CC} = 5.0V, V_O = 0.4V	3.75			3.0	6.0		2.1			mA
	V_{CC} = 10V, V_O = 0.5V	10			8.0	16		5.6			mA
Output Drive Current P-Channel (I_DP)	V_{CC} = 5.0V, V_O = 4.5V	−0.62			−0.5	−1.0		−0.35			mA
	V_{CC} = 5.0V, V_O = 2.5V	−1.85			−1.25	−2.5		−0.9			mA
	V_{CC} = 10V, V_O = 9.5V	−1.85			−1.25	−2.5		−0.9			mA
Input Current (I_I)	V_{IH} = V_{CC}					10					pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

dynamic electrical characteristics MM4650AD, MM4650AF, MM5650AF

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical Temperature Coefficient for all values of $V_{CC} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High-to-Low Level (t_{PHL})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		55	110	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		25	55	ns
Propagation Delay Time Low-to-High Level (t_{PLH})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		90	140	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		40	85	ns
Transition Time High-to-Low Level (t_{THL})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		20	45	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		16	40	ns
Transition Time Low-to-High Level (t_{TLH})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		50	100	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		30	60	ns
Input Capacitance (C_I)	Any Input		5.0		pF

dynamic electrical characteristics MM4649AD, MM4649AF, MM5649AN

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical Temperature Coefficient for all values of $V_{CC} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High-to-Low Level (t_{PHL})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		15	55	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		10	30	ns
Propagation Delay Time Low-to-High Level (t_{PLH})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		50	80	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		25	55	ns
Transition Time High-to-Low Level (t_{THL})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		20	45	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		16	40	ns
Transition Time Low-to-High Level (t_{TLH})	$V_{CC} = 5.0V$, $V_{IH} = V_{CC}$		50	100	ns
	$V_{CC} = 10V$, $V_{IH} = V_{CC}$		30	60	ns
Input Capacitance (C_I)	Any Input		5.0		pF

MM14511 BCD-to-seven segment latch/decoder/driver

general description

The MM14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

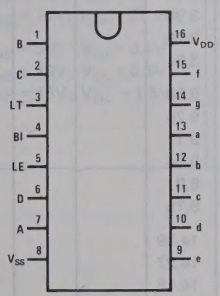
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

features

- Low logic circuit power dissipation
- High current sourcing outputs (up to 25 mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility

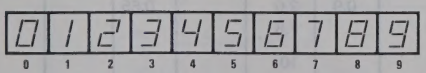
connection diagram

Dual-In-Line Package



TOP VIEW

Display



Segment Identification

truth table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't care

*Depends upon the BCD code applied during the 0 to 1 transition of LE.

absolute maximum ratings

Voltage at Any Pin (Note 1)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	
MM14511AD	−55°C to +125°C
MM14511CN	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics MM14511AD

PARAMETER	CONDITIONS	−55°C			+25°C			+125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V					14.59					V
Noise Immunity (V_{NL})	V_{DD} = 5V, $V_{OUT} \geq 3.5V$	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, $V_{OUT} \geq 7V$	3.0			3.0	4.5		2.9			V
	V_{DD} = 15V, $V_{OUT} \geq 10.5V$					6.75					V
Noise Immunity (V_{NH})	V_{DD} = 5V, $V_{OUT} \leq 1.5V$	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, $V_{OUT} \leq 3V$	2.9			3.0	4.5		3.0			V
	V_{DD} = 15V, $V_{OUT} \leq 4.5V$					6.75					V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA				4.1	4.57					V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA				3.9	4.12					V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA				3.4	3.75					V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA				9.1	9.58					V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA				9.0	9.17					V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA				8.6	8.9					V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA					14.59					V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA					14.18					V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA					13.95					V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Output (Sink) Drive Voltage (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.5			0.4	0.78		0.28			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.1			0.9	2.0		0.65			mA
	V_{DD} = 15V, V_{OL} = 1.5V					7.8					mA
Input Current (I_{IN})						10					pA

Note 1: Devices should not be connected with power on.

dc electrical characteristics MM14511CN

PARAMETER	CONDITIONS	−40°C			+25°C			+85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V					14.59					V
Noise Immunity (V_{NL})	V_{DD} = 5V, $V_{OUT} \geq$ 3.5V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, $V_{OUT} \geq$ 7V	3.0			3.0	4.5		2.9			V
	V_{DD} = 15V, $V_{OUT} \geq$ 10.5V					6.75					V
Noise Immunity (V_{NH})	V_{DD} = 5V, $V_{OUT} \leq$ 1.5V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, $V_{OUT} \leq$ 3V	2.9			3.0	4.5		3.0			V
	V_{DD} = 15V, $V_{OUT} \leq$ 4.5V					6.75					V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA				4.1	4.57					V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA				3.6	4.12					V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA				2.8	3.75					V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA				9.1	9.58					V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA				8.75	9.17					V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA				8.1	8.9					V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA					14.59					V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA					14.18					V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA					13.95					V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Output (Sink) Drive Voltage (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.23			0.2	0.78			0.16		mA
	V_{DD} = 10V, V_{OL} = 0.5V	0.6			0.5	2.0			0.4		mA
	V_{DD} = 15V, V_{OL} = 1.5V					7.8					mA
Input Current (I_{IN})						10					pA

ac electrical characteristics

$T_A = 25°C$ and $C_L = 15$ pF, typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

PARAMETER	CONDITIONS	MM14511AD			MM14511CN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Capacitance (C_{IN})	$V_{IN} = 0$		5.0			5.0		pF
Output Rise Time (t_r) (*Figure 1a*)	$V_{DD} = 5.0V$		30	175		30	200	ns
	$V_{DD} = 10V$		17	75		17	110	ns
	$V_{DD} = 15V$		15			15		ns
Output Fall Time (t_f) (*Figure 1a*)	$V_{DD} = 5.0V$		1000			1000		ns
	$V_{DD} = 10V$		1000			1000		ns
	$V_{DD} = 15V$		1000			1000		ns
Turn-Off Delay Time (Data) (t_{PLH}) (*Figure 1a*)	$V_{DD} = 5.0V$		640	1500		640	2250	ns
	$V_{DD} = 10V$		250	600		250	900	ns
	$V_{DD} = 15V$		175			175		ns
Turn-On Delay Time (Data) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		720	1500		720	2250	ns
	$V_{DD} = 10V$		290	600		290	900	ns
	$V_{DD} = 15V$		195			195		ns
Turn-Off Delay Time (Blank) (t_{PLH}) (*Figure 1a*)	$V_{DD} = 5.0V$		320	1000		320	1500	ns
	$V_{DD} = 10V$		130	400		130	600	ns
	$V_{DD} = 15V$		100			100		ns
Turn-On Delay Time (Blank) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		485	1000		485	1500	ns
	$V_{DD} = 10V$		200	400		200	600	ns
	$V_{DD} = 15V$		160			160		ns
Turn-Off Delay Time (Lamp Test) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		290	625		290	940	ns
	$V_{DD} = 10V$		125	250		125	375	ns
	$V_{DD} = 15V$		85			85		ns
Turn-On Delay Time (Lamp Test) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		290	625		290	940	ns
	$V_{DD} = 10V$		120	250		120	375	ns
	$V_{DD} = 15V$		90			90		ns
Setup Time (t_{SETUP}) (*Figure 1b*)	$V_{DD} = 5.0V$	180	90		270	90		ns
	$V_{DD} = 10V$	76	38		114	38		ns
	$V_{DD} = 15V$		20			20		ns
Hold Time (t_{HOLD}) (*Figure 1b*)	$V_{DD} = 5.0V$	0	−90		90	−90		ns
	$V_{DD} = 10V$	0	−38		38	−38		ns
	$V_{DD} = 15V$		−20			−20		ns
Minimum Latch Enable Pulse Width (PW_{LE}) (*Figure 1c*)	$V_{DD} = 5.0V$	520	260		780	260		ns
	$V_{DD} = 10V$	220	110		330	110		ns
	$V_{DD} = 15V$		65			65		ns

switching time waveforms

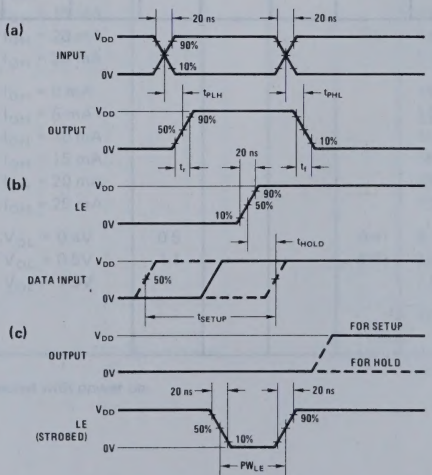
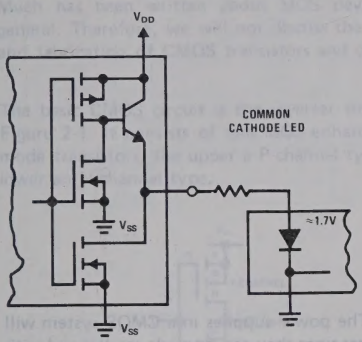
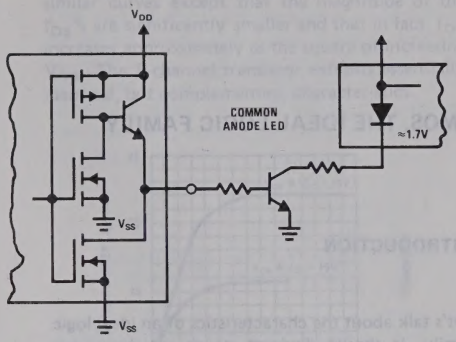


FIGURE 1.

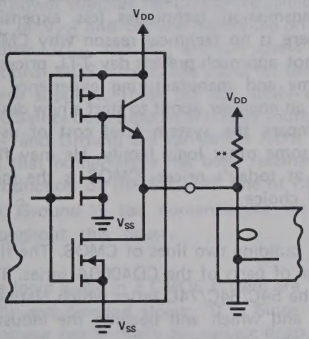
typical applications

Light Emitting Diode (LED) Readout



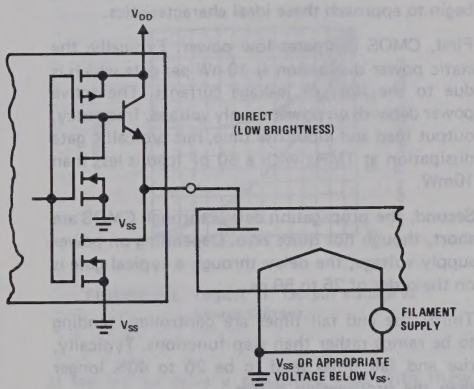


Incandescent Readout

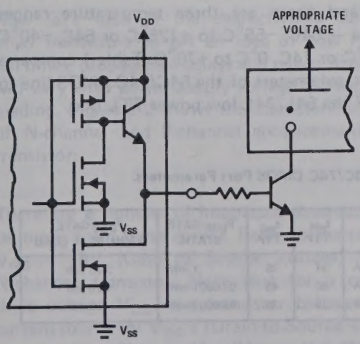


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

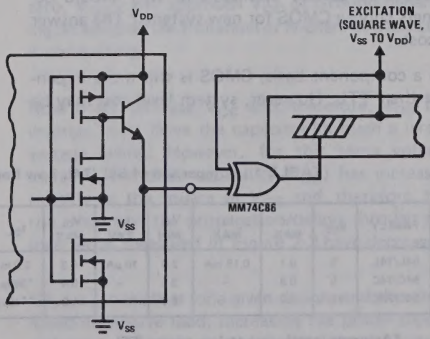
Flourescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

Stephen Calebotta
National Semiconductor

CMOS, THE IDEAL LOGIC FAMILY

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

Well, that ideal logic family is here — almost. The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50 pF load is less than 10mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/64C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/64C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are three temperature ranges available — 54C, −55°C to +125°C or 64C, −40°C to +80°C or 74C, 0°C to +70°C. Table 1 compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

TABLE 1. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters.

FAMILY	V_{CC}	V_{IL} MAX	I_{IL} MAX	V_{IH} MIN	I_{IH} 2.4V	V_{OL} MAX	I_{OL}	V_{OH} MIN	I_{OH}	t_{pd0} TYP	t_{pd1} TYP	P_{DISS}/GATE STATIC	P_{DISS}/GATE 1 MHz, 50 pF LOAD
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	–	3.5	–	0.4	*360μA	2.4	*100μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	–	8.0	–	1.0	**10μA	9.0	**10μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.

**Assumes interfacing to CMOS.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 2-1. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.

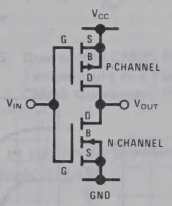


FIGURE 2-1. Basic CMOS Inverter.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomeclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.

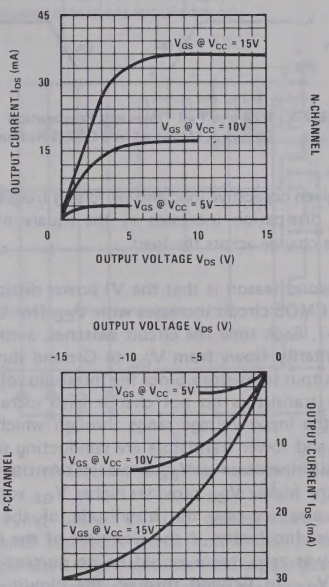


FIGURE 2-2. Logical "1" Output Voltage vs Source Current.

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system.

Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.

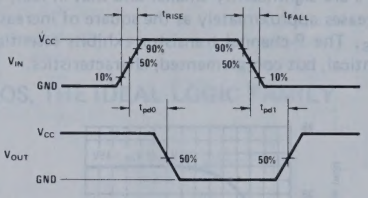


FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System.

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them giving the rounded characteristic.

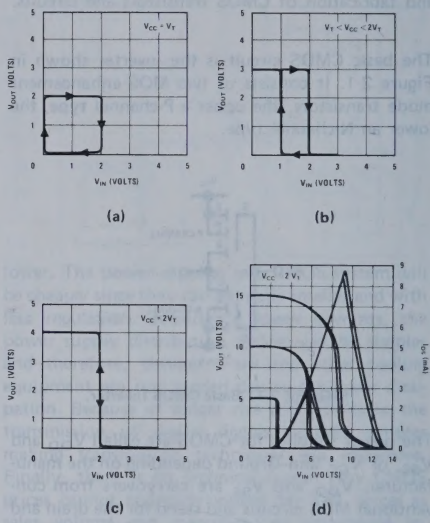


FIGURE 2-4. Transfer Characteristics vs V_{CC}.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input

can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:

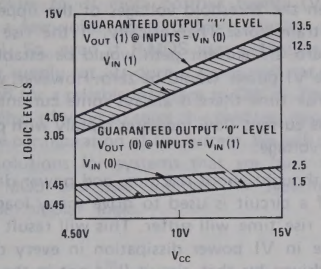


FIGURE 2-5. Guaranteed CMOS DC Margin Over Temperature as a Function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

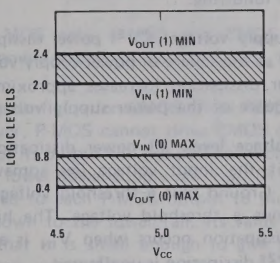


FIGURE 2-6. Guaranteed TTL DC Margin Over Temperature as a Function of V_{CC}. TTL Guarantees 0.4V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A & B be the unused inputs.

If we were going to tie the unused inputs to a logic level, inputs A & B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

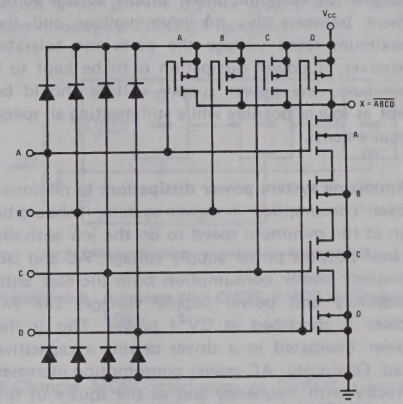


FIGURE 3-1. MM74C20 Four Input NAND Gate.

So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

Parallel gates: depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 3-2. This insures that there are a number of parallel combinations of the series string of transistors (Figure 3-1), thereby increasing drive in that direction also.

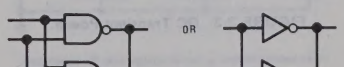


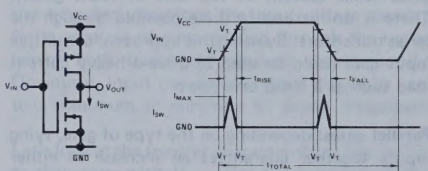
FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: there are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (part no. MM5616A). Second,

and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

Power supply filtering: since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: to minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) Figure 3-3.



VI POWER IS GIVEN BY:

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times \text{RISE TIME TO PERIOD RATIO}$$

$$\text{RISE TIME TO PERIOD RATIO} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{WHERE } \frac{1}{t_{TOTAL}} = \text{FREQUENCY}$$

$$P_{VI} = 1/2\,(V_{CC} - 2V_T)\, I_{CC\,MAX}\, (t_{RISE} + t_{FALL})\, \text{FREQ.}$$

FIGURE 3-3. DC Transient Power.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See Figure 2-4d.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at 1/2 V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** the CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: there are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17 to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem

is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

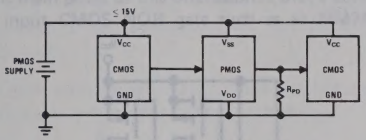
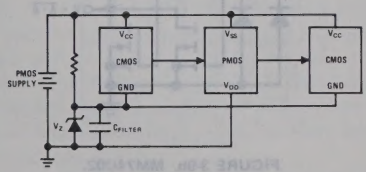


FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS.

First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, Figure 3-4.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, Figure 3-5.

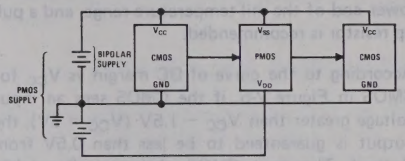


Use a bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where The P-MOS Supply is Greater Than 15V.

In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, Figure 3-6.

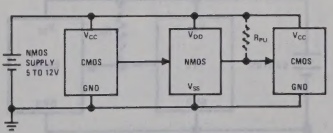


Run the CMOS from the bipolar supply and interface directly to P-MOS

FIGURE 3-6. A System With CMOS, P-MOS and Bipolar Logic.

N-Channel MOS: interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower power supply rail to about 1 to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output level will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



Both operate off same supply with pull up resistors optional from N-MOS to CMOS.

FIGURE 3-7. A System With CMOS and N-MOS Only.

TTL, LPTTL, DTL: two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

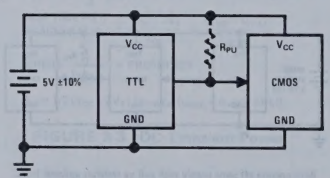
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the mil temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the mil temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable (V_{CC} = 4.5V).

Under nominal conditions (25°C, V_{IN} = 0.4V, nominal leakage currents into CMOS and V_{CC} = 5V) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times −2mV per °C, or −4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface.

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360μA (about 420μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

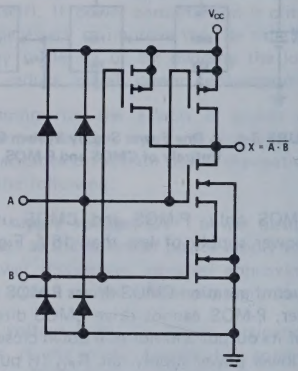


FIGURE 3-9a. MM74C00.

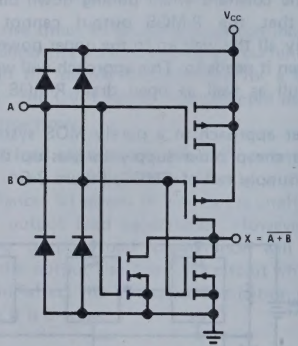


FIGURE 3-9b. MM74C02.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum

spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360μA is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 and 540μA (between 2 and 3 LPTTL input loads). The 360μA sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

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National Semiconductor

CMOS LINEAR APPLICATIONS

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

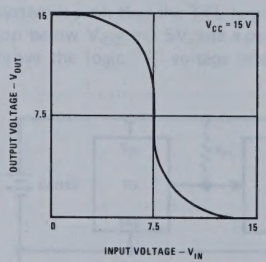


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

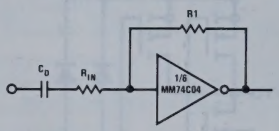


FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

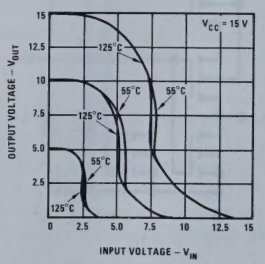


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

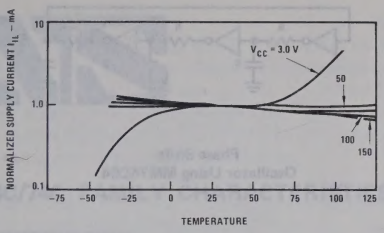


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

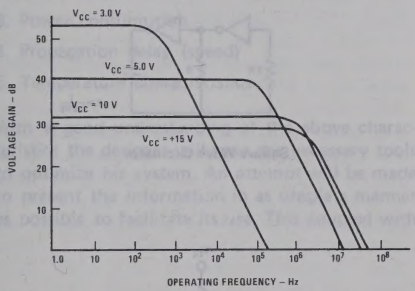


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

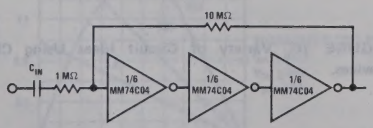


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

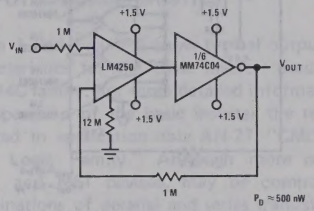


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

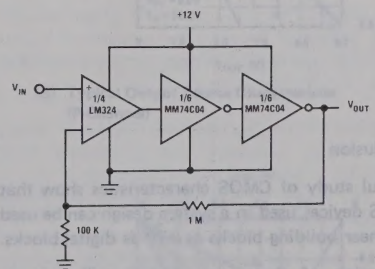


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA

from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

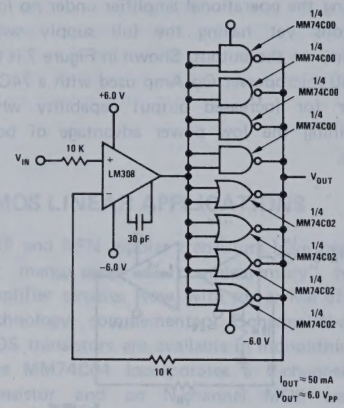


FIGURE 9. MM74C00 and MM7402 Used as a Post Amplifier to Provide Increased Current Drive.

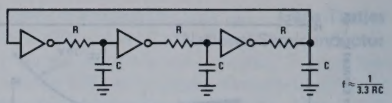
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

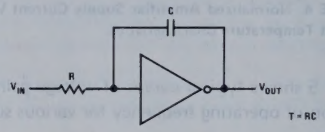
Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

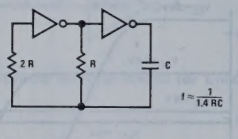
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



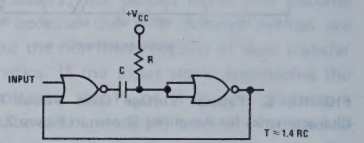
Phase Shift
Oscillator Using MM74C04



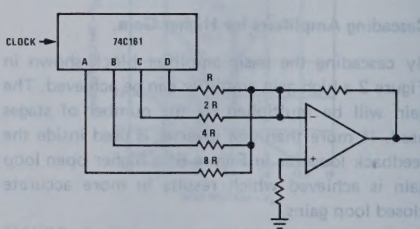
Integrator Using
Any Inverting CMOS Gate



Square Wave Oscillator



One Shot



Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

Thomas P. Redfern
National Semiconductor

54C/74C FAMILY CHARACTERISTICS

INTRODUCTION

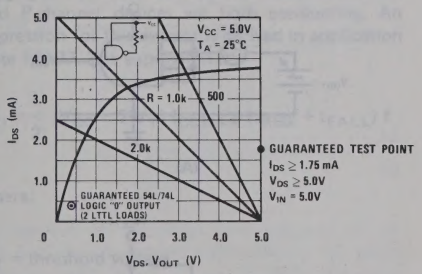
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

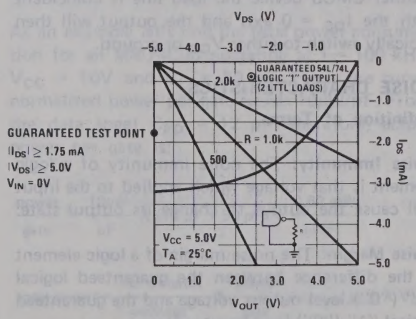
With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

Figure 1 and Figure 2 show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to application note AN-77, "CMOS, The Ideal Logic Family." Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.

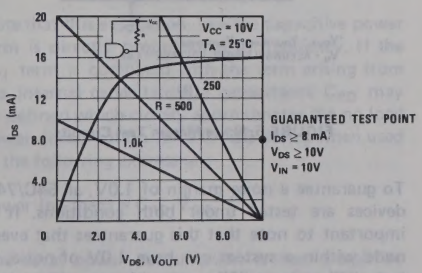


(A) Typical Output Sink Characteristic (N-Channel)

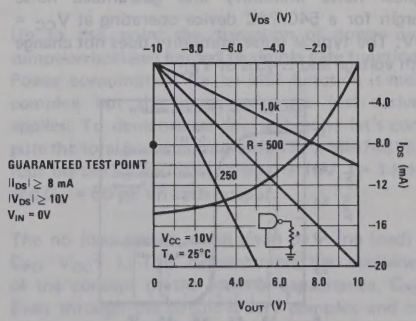


(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)



(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see Figures 1 and 2). These points are:

V_{CC} = 5.0V	V_{IN} = 5.0V $I_{DS} \geq$ 1.75 mA $V_{DS} \geq$ 5.0V	V_{IN} = 0V $\|I_{DS}\| \geq$ 1.75 mA $\|V_{DS}\| \geq$ 5.0V
V_{CC} = 10V	V_{IN} = 10V $I_{DS} \geq$ 8.0 mA $V_{DS} \geq$ 10V	V_{IN} = 0V $\|I_{DS}\| \geq$ 8.0 mA $\|V_{DS}\| \geq$ 10V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. Figures 1 and 2 show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of Figure 3 shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

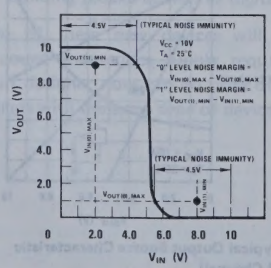


FIGURE 3. Typical Transfer Characteristic

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see Figure 4).

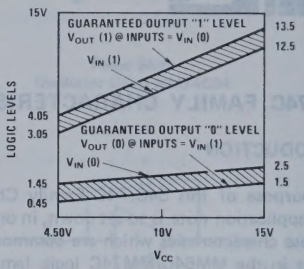
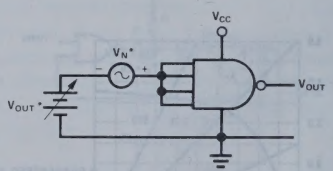


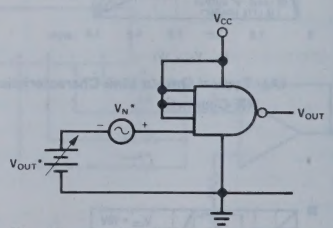
FIGURE 4. Guaranteed Noise Margin Over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. Figure 5 indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.



(A)



*V_{OUT} = $V_{OUT(1)MIN}$, $V_{OUT(0)MAX}$
V_N = ALLOWABLE NOISE VOLTAGE = 1.0V

(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in Figure 5.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current (2) transient power due to load capacitance (3) transient power due to internal capacitance and (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is 1/2 CV^2. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then 2 [(1/2) CV_{CC}^2] = CV_{CC}^2. Energy per unit time, or power, is then CV_{CC}^2 f, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in application note AN-77. The expression is:

$$P_{VI} = \frac{1}{2} (V_{CC} - 2\ V_T)\ I_{CCMAX}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

$$\text{Power (no load)} = C_{PD}\ V_{CC}^2\ f$$

The total power consumption is then simplified to:

$$\text{Total Power} = (C_{PD} + C_L)\ V_{CC}^2\ f + I_{LEAK}\ V_{CC} \quad (1)$$

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further Figure 6 gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

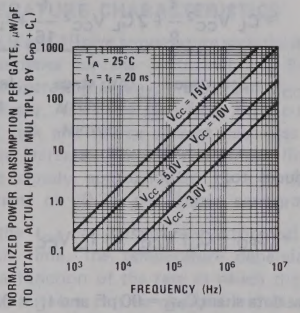


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\mu W}{pF} \times (12\ pF + 50\ pF) = \frac{0.62\ mW}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ mW + 0.01\mu A \times 10V \cong 2.48\ mW$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}^2$ f. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even through the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD} V_{CC}^2 f}_{\text{no load power}} + \underbrace{C_L V_{CC}^2 \frac{f}{2}}_{\text{output power of 1st stage}} + \underbrace{C_L V_{CC}^2 \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L V_{CC}^2 \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2 C_L V_{CC}^2 \frac{f}{16}}_{\text{4th stage \& carry output}} + \underbrace{I_L V_{CC}}_{\text{leakage term}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L) V_{CC}^2 f + I_L V_{CC}$$

From the data sheet C_{PD} = 90 pF and I_L = 0.05μA. Using Figure 6 total power is then:

$$P_{TOTAL} = (90\ pF + 50\ pF) \times \frac{100\mu W}{pF} + 0.05 \times 10^{-6} \times 10V \cong 14\ mW$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of Figure 6 and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF and input rise and fall times of 20 ns. A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem Figure 7 has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because

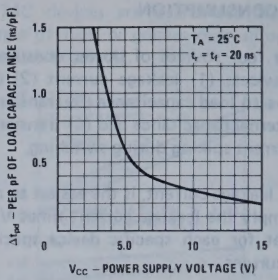


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

$$t_{pd}\Big|_{C_L = C} = (C - 50)\ pF \times \frac{\Delta t_{pd}}{pF} + t_{pd}\Big|_{C_L = 50\ pF}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\ pF}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{pF}$ = Value obtained from Figure 7.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\ pF} = (15 - 50)\ pF \times 0.57 \frac{ns}{pF} + 50\ ns$$

$$= -20\ ns + 50\ ns = 30\ ns$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\ pF} = (100 - 50)\ 0.29\ ns + 70\ ns$$

$$= 14.5 + 70 \cong 85\ ns$$

It is significant to note that this equation and Figure 7 apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller $\Delta t_{pd}/pF$.

Another point to consider in the design of a CMOS system is the affect of power supply voltage on propagation delay. Figure 8 shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

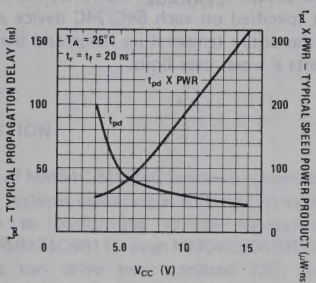


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

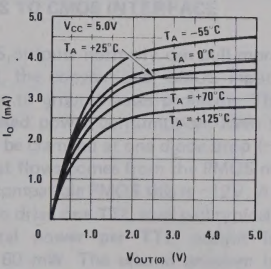
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out." Going from V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%. Clearly for $V_{CC} > 10V$ a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However in general it can be seen from Figure 8 that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

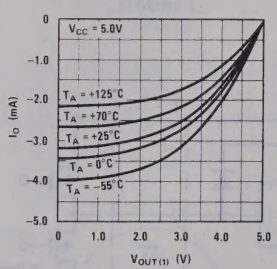
TEMPERATURE CHARACTERISTICS

Figures 9 and 10 give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The affect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependance of t_{pd} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.

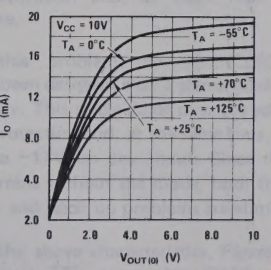


(A) Typical Output Drain Characteristic (N-Channel)

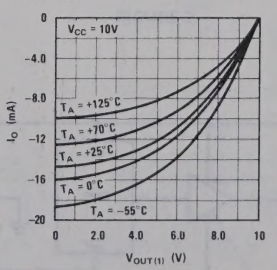


(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



(A) Typical Output Drain Characteristic (N-Channel)



(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10

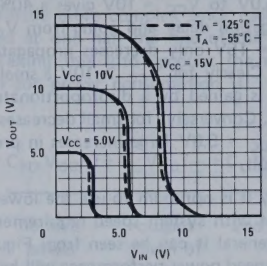


FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of Figure 9 and 10 show considerable variation with temperature. Examination of the transfer characteristics of Figure 11 indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independance of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

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Thomas P. Redfern
National Semiconductor

MM54C/MM74C VOLTAGE TRANSLATION/BUFFERING

INTRODUCTION

A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at V_{CC} = 5V. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

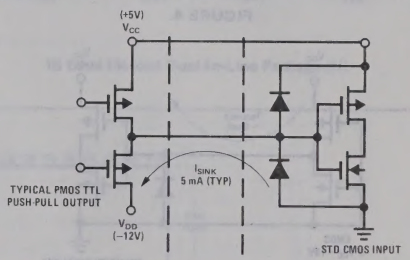


FIGURE 1.

MM74C901 PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

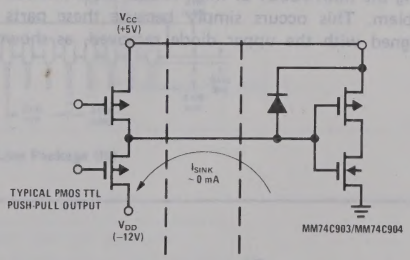


FIGURE 2.

To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2, and 3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.

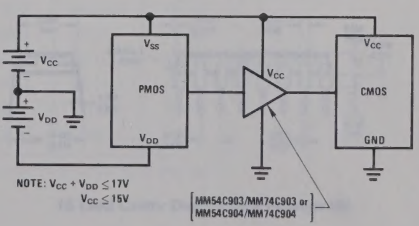


FIGURE 3. PMOS to CMOS or TTL Interface

CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4.* Again, this will cause increased power as well as possible four layer diode action.

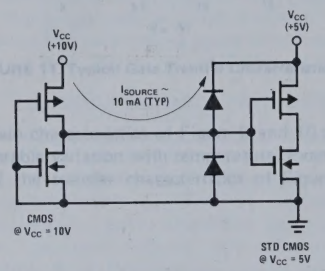


FIGURE 4.

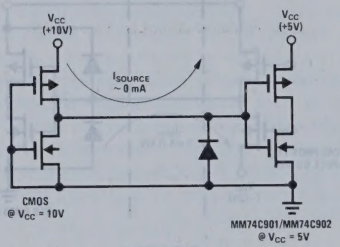


FIGURE 5.

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5.* With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.

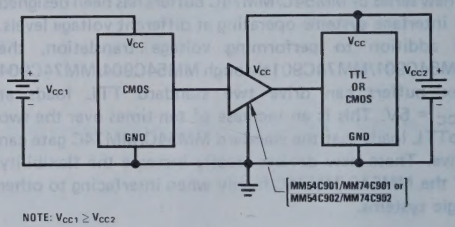
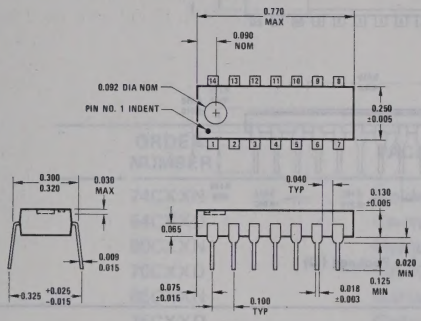


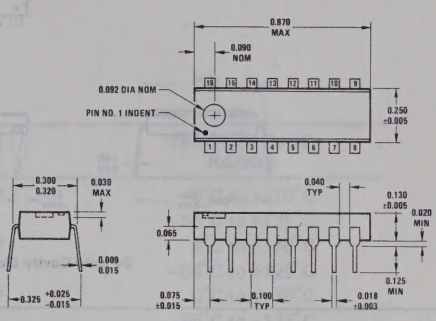
FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.

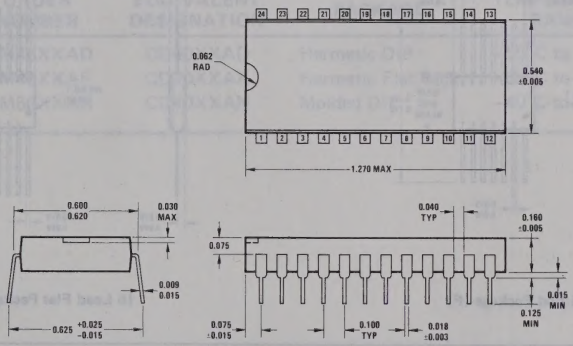
CMOS PACKAGES



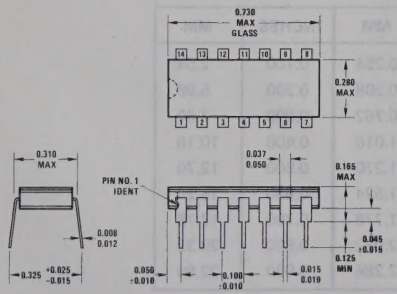
14 Lead Molded Dual-In-Line Package (N)



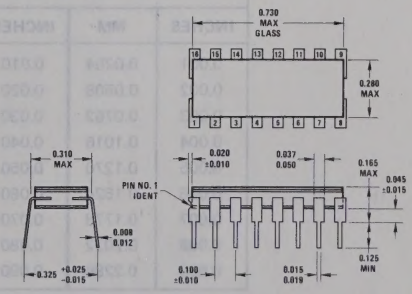
16 Lead Molded Dual-In-Line Package (N)



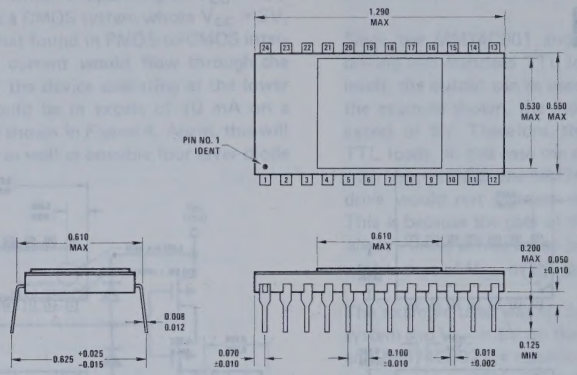
24 Lead Molded Dual-In-Line Package (N)



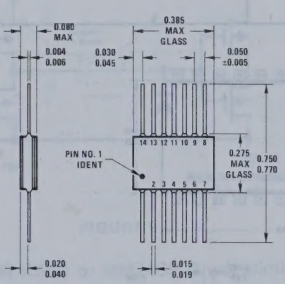
14 Lead Cavity Dual-In-Line Package (D)



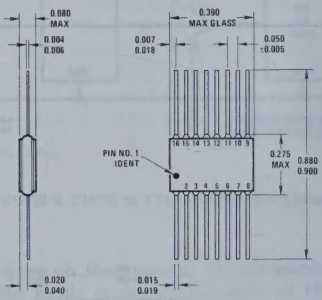
16 Lead Cavity Dual-In-Line Package (D)



24 Lead Cavity Dual-In-Line Package (D)



14 Lead Flat Package (F)



16 Lead Flat Package (F)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

All package dimensions are in inches.

ORDERING INFORMATION

ORDER NUMBER	PACKAGE	TEMPERATURE RANGE
74CXXN	Molded DIP	0°C to + 70°C
54CXXD	Cavity DIP	−55°C to +125°C
80CXXN	Molded DIP	0°C to + 70°C
70CXXD	Cavity DIP	−55°C to +125°C
85CXXN	Molded DIP	0°C to + 70°C
75CXXD	Cavity DIP	−55°C to +125°C

ORDER NUMBER	EQUIVALENT DESIGNATION	PACKAGE	TEMPERATURE RANGE
MM46XXAD	CD40XXAD	Hermetic DIP	−55°C to +125°C
MM46XXAF	CD40XXAK	Hermetic Flat Pack	−55°C to +125°C
MM56XXAN	CD40XXAN	Molded DIP	−40°C to + 85°C

ORDER NUMBER	PACKAGE	TEMPERATURE RANGE
74CXXN	Molded DIP	0°C to + 70°C
84CXXD	Cavity DIP	−55°C to +125°C
80CXXN	Molded DIP	0°C to + 70°C
70CXXD	Cavity DIP	−55°C to +125°C
80CXXN	Molded DIP	0°C to + 70°C
75CXXD	Cavity DIP	−55°C to +125°C

ORDER NUMBER	EQUIVALENT DESIGNATION	PACKAGE	TEMPERATURE RANGE
MM5XXAD	CD4XXAD	Hermetic DIP	−55°C to +125°C
MM5XXAE	CD4XXAE	Hermetic Flat Package	−55°C to +125°C
MM5XXAN	CD4XXAN	Molded DIP	−40°C to +85°C

INCHES TO MILLIMETER CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

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